# BUDDHA SERIES

## (Unit Wise Solved Question & Answers)

## Course – B.Tech (ECE)

## College – Buddha Institute of Technology

**(AKTU CODE-525)**

## Department: ELECTRONICS & COMMUNICATION ENGINEERING

## Subject: VLSI TECHNOLOGY (BEC054)

## Faculty Name: Mr. Anil Chaudhary

## Unit – 1-5

**Q 1.** Define the term IC. List its types?

**Ans.** An integrated circuit (**IC**), sometimes called a chip or microchip, is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, and transistors are fabricated. An **IC can** function as an amplifier, oscillator, timer, counter, computer memory, or microprocessor.

**OR**

It is the combination of active & passive elements, when placed on the same substrate, usually Si Active elements are those, which can produce gain or can amplify signals, like transistors or amplifiers. Passive elements doesn't have this kind of capability without active elements, like resistors capacitors, inductors

There are 3 ways to classify Integrated Circuits.

1. On the basis of fabrication techniques used
2. On the basis of the chip size
3. On the basis of applications

**Q 2.** What does Moore's law state? AKTU-2022-23

**Ans. Moore's Law –**

Gordon Moore, in 1965 an integrated circuit pioneer and cofounder of Intel corporation predicted that, the number of transistors on chip will be double by every 18 months.

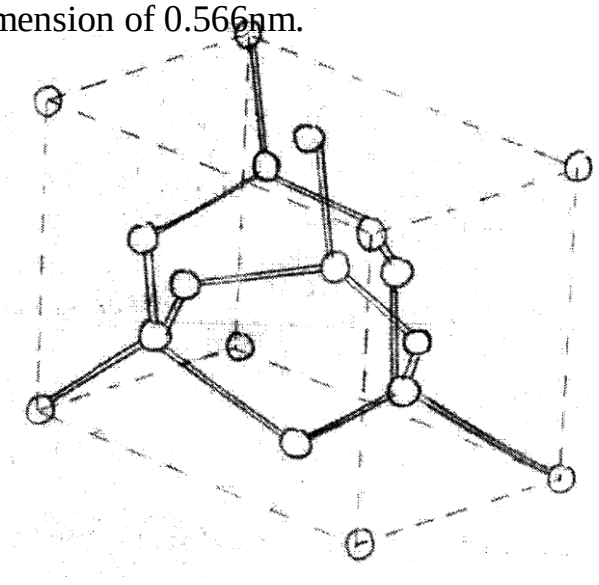
**Q 3.** List two major defect that appear in crystal structure? AKTU-2022-23

Ans. Real crystals have defects classified as follows:

(1)point defect, (2) line defect, (3) area or planar defect, and (4) volume defect. Defectsinfluence the optical, electrical, and mechanical properties of silicon.

**Q 4.** Define the crystal structure of Silicon. AKTU-2020-21

**Ans. Crystal Structure :** Silicon structure in the same pattern as diamond in a structure which aschroft and Mermin call two interpenetrating face – centered cubic primitive lattice. The line between silicon atoms in the lattice illustration indicates nearest neighbour bonds. The cube side for silicon is 0.543nm. Germanium has same diamond structure with cell dimension of 0.566nm.



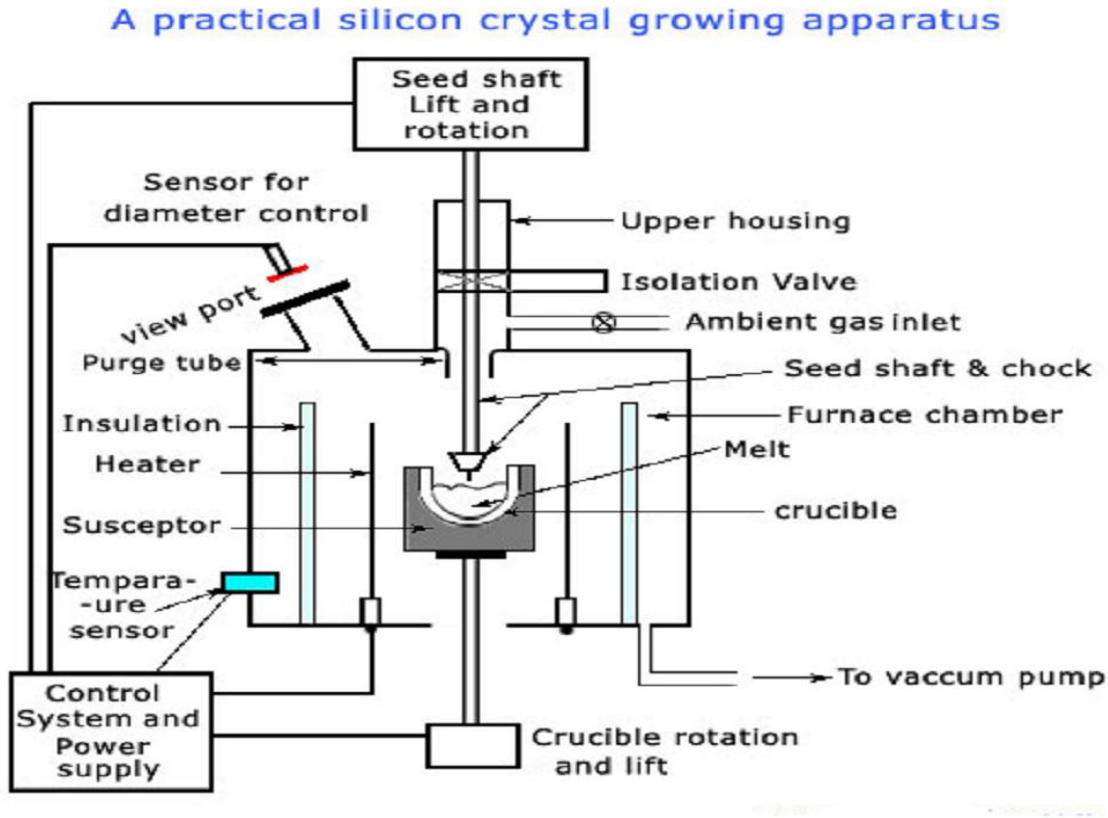
**Q 5** .What are point defects? AKTU-2020-21

**Ans. Point Defects:** Point defects are localized disruptions in the regular atomic arrangement of a crystal lattice. They can include:

- **Vacancies:** Vacancies are empty spaces in the crystal lattice where an atom is missing. They can occur due to thermal fluctuations or during crystal growth.
- **Interstitials:** Interstitials are atoms or ions that occupy positions in the crystal lattice that are not part of the regular lattice sites. This can result in distortion of the lattice structure.
- **Substitutional Defects:** In substitutional defects, one type of atom is replaced by another type of atom in the crystal lattice. This can lead to changes in the material's properties, such as electrical conductivity or mechanical strength.

**Q 6.** Describe CZ process in detail with neat diagram. Mention the importance of inert ambient during the process. AKTU-2020-21,21-22,22-23

**Ans.** The highly refined silicon (EGS) though free from impurities, is still polycrystalline. Hence it is to be processed to become single crystal. The Czochralski crystal growth process is often used for producing single-crystal silicon ingots. The diagram is given below.




**Czochralsky Process Apparatus**

Since monolithic ICs are usually fabricated on a substrate which is doped with impurity, the poly-crystalline silicon with an appropriate amount of dopant is-put into a quartz crucible, which is then placed inside a crystal growth furnace. The material is then heated to a temperature that is slightly in excess of the silicon melting pint of 1420

degree Celsius. A small single-crystal rod of silicon called a seed crystal is then dipped into the silicon melt. The conduction of heat up the seed crystal will produce a reduction in the temperature of the melt in contact with the seed crystal to slightly below the silicon melting point. The silicon will therefore freeze onto the end of the seed crystal, and as the seed crystal is slowly pulled up out of the melt it will pull up with it a solidified mass of silicon that will be a crystallographic continuation of the seed crystal. Both the seed crystal and the crucible are rotated but in opposite directions during the crystal pulling process in order to produce crystalline ingots of circular cross section. The liquid solid interface remains near to the surface of the melt if the temperature and pulling rate are correctly chosen. Even a long single crystal silicon is pulled from it. The diameter of the ingot is controlled by the pulling rate and the melt temperature, with ingot diameters of about 100 to 150 mm (4 to 6 inches) being the most common. The ingot length will generally be of the order of 3 meter, and several hours are required for the "pulling" of a complete ingot. The crystal pulling is done in an inert-gas atmosphere (usually argon or helium), and sometimes a vacuum is used. This is done to prevent oxidation" The pull-rate is closely related to the heat input and losses, crystal properties and dimensions. The conditions for crystal pulling are therefore carefully controlled. For example, the melt temperature is monitored with a thermocouple and feedback controller. Longer diameter crystals have commercial advantages and can be grown. However, difficulties may be encountered because of resistivity gradient across finished slices. The crystal growth apparatus shown in the figure above consists of the following parts.

- Furnace
- Crystal pulling mechanism
- Ambient control facility
- Control system circuitry

The furnace consists of a crucible, susceptor (crucible support) and rotational mechanism, heating element and power supply, and a chamber. As the crucible contains the melt, it is the most important component of the growth apparatus. The crucible material should be chemically unreactive with molten silicon. Also, the material should have high melting point, thermal stability, and hardness. The materials for crucible, which satisfy these properties, are silicon nitride ($Si_3N_4$) and fused silica ($SiO_2$). The latter is in exclusive use nowadays. Fused silica; however, reacts with silicon, releasing silicon and oxygen into the melt. In tins process the crucible undergoes erosion. The susceptor, is used to support the silica crucible. It also provides for better thermal conditions. Graphite is the material of choice because of its hightemperature properties. The graphite should be pure to prevent contamination of the crystal from impurities that would be volatilized from the graphite at the temperature involved. The susceptor rests on a pedestal whose shaft is connected to a motor that provides rotation. The whole assembly can usually be raised and lowered to keep the melt level equidistant from a fixed reference point, which is needed for automatic diameter control. The chamber housing the furnace must provide easy access to the furnace components to facilitate

maintenance and cleaning. The furnace structure must be airtight to prevent contamination from the atmosphere, and have a specific design that does not allow any part of the chamber to become so hot that its vapour pressure would be a factor in contaminating the crystal. Hottest parts of the apparatus are water cooled Insulation is usually provided between the heater and the chamber wall. The crystal-pulling mechanism consists of seed shaft or chain, rotation mechanism, and seed chuck. The mechanism controls two parameters of die growth process: pull rate and crystal rotation. Also, the pulling mechanism must have minimum vibration and great precision.
The seed holder and pulling mechanism must maintain precise orientation perpendicular to the melt surface.
From the figure shown below you can see that the crystal leaves the furnace through a purge tube, where ambient gas, if present, is directed along the surface of the crystal to cool it. From the purge tube, the crystal enters an upper chamber, which is usually separated from the furnace by an isolation valve. The ambient control for the crystal growth apparatus consists of gas source, flow control, purge lube, and exhaust or vacuum system. The crystal growth must be conducted in an inert gas or vacuum as staled earlier. This is necessary because

- The hot graphite parts must be protected from oxygen to prevent erosion and
- The gas around the process should not react with the molten silicon. Growth in vacuum meets these requirements.

Growth in a gaseous atmosphere, generally used on large growers, must use an inert gas such as helium or argon. The inert gas may be at atmospheric pressure or at reduced pressure. The control system for crystal growing may consist of micro processing sensors, and outputs and provides control of process parameters such as temperature, crystal diameter, pull rate and rotation speed. The use of digital or microprocessor-based systems for control is more common because these rely less on operator intervention and have many parts of the process pre-programmed.

**Q 7.** Explain production process of Electronic Grade Silicon from silica with neat diagram. AKTU-2020-21

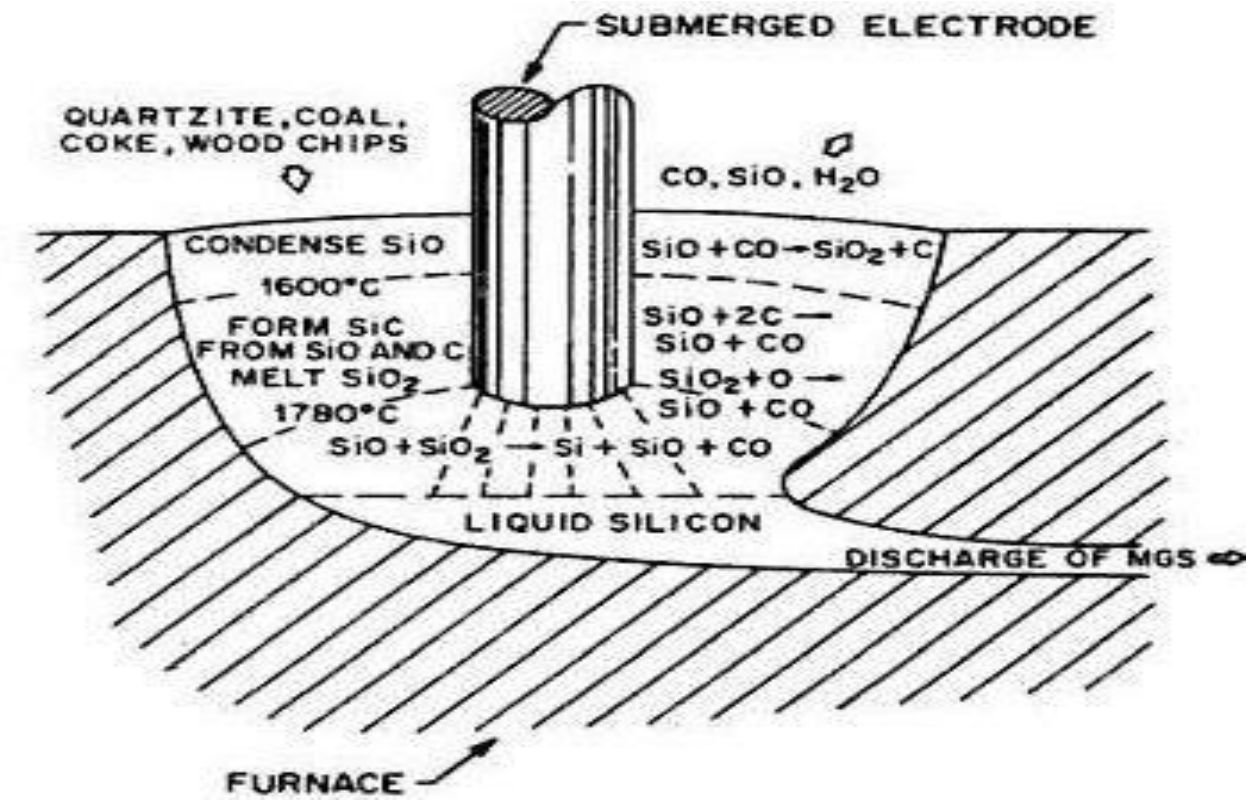
**Electronic Grade Silicon (EGS)-**

Silicon occurs naturally in form of silica and silicates. It is most important semiconductor for the electronic industry. More than 95% semiconductor devices are made of silicon. It is easy to grow $SiO_2$.
Electronic-grade silicon (EGS), a polycrystalline material of high purity, is the raw material for the preparation of single-crystal silicon. EGS is undoubtedly one of the purest materials routinely available. The pure EGS will have doping elements in the parts per billion (ppb) range, and carbon less than 2 part per million The step by step procedure regarding the production of EGS is shown in the block diagram.

**Production of EGS**

The process starts by the production of Metallurgical Grade Silicon (MGS) by charging it with quartzite and carbon in an arc furnace. Quartzite is a relatively pure form of sand (SiQ2), and carbon is obtained in the form of coal, coke, and wood chips.
The overall reaction in the furnace is given below.

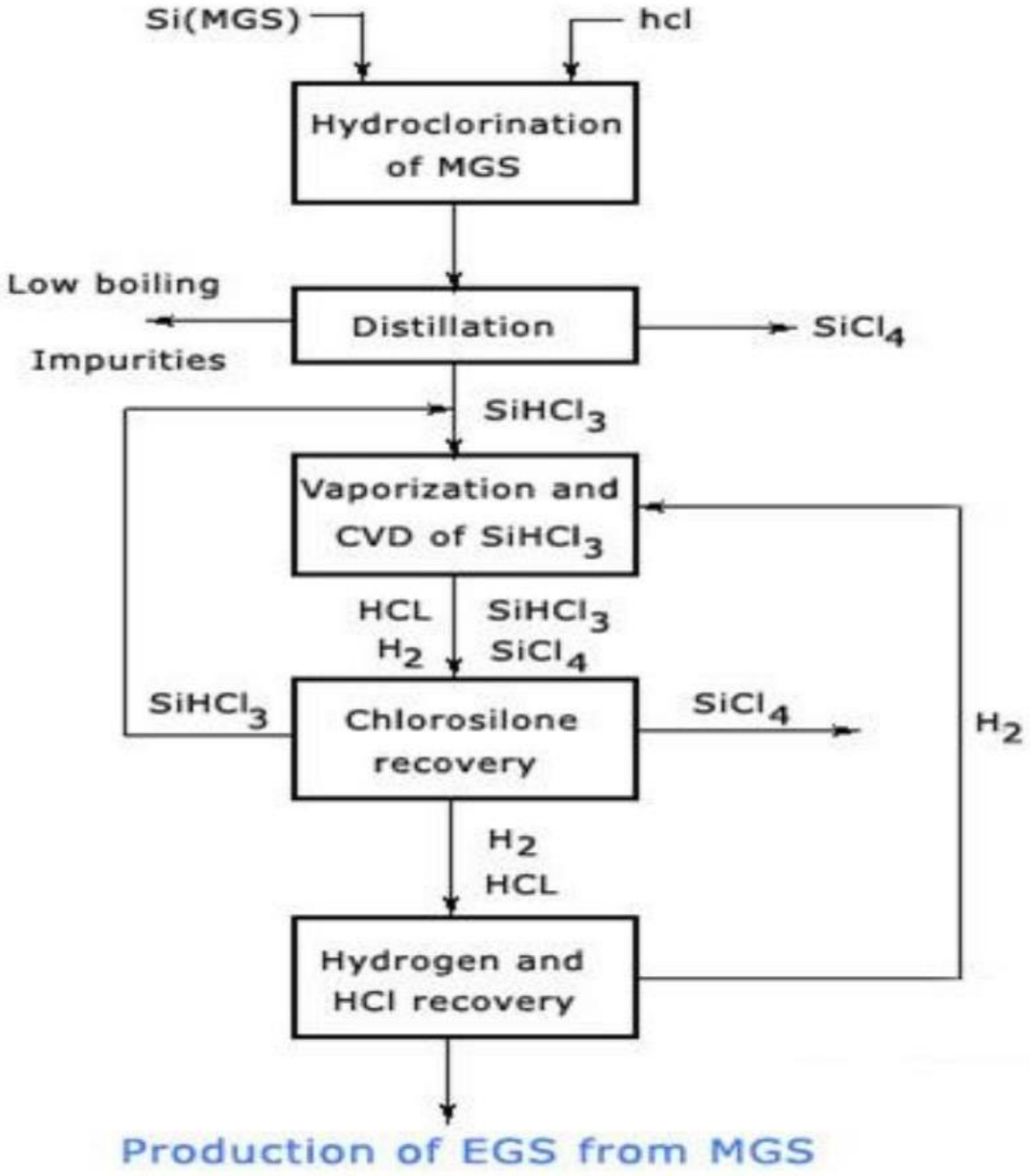
**SiC (solid) + Si02 (solid) = Si (solid)+ SiO (gas) + CO (gas)**




**Schematic of a submerged-electrode arc furnace for the production of metallurgical-grade silicon.**

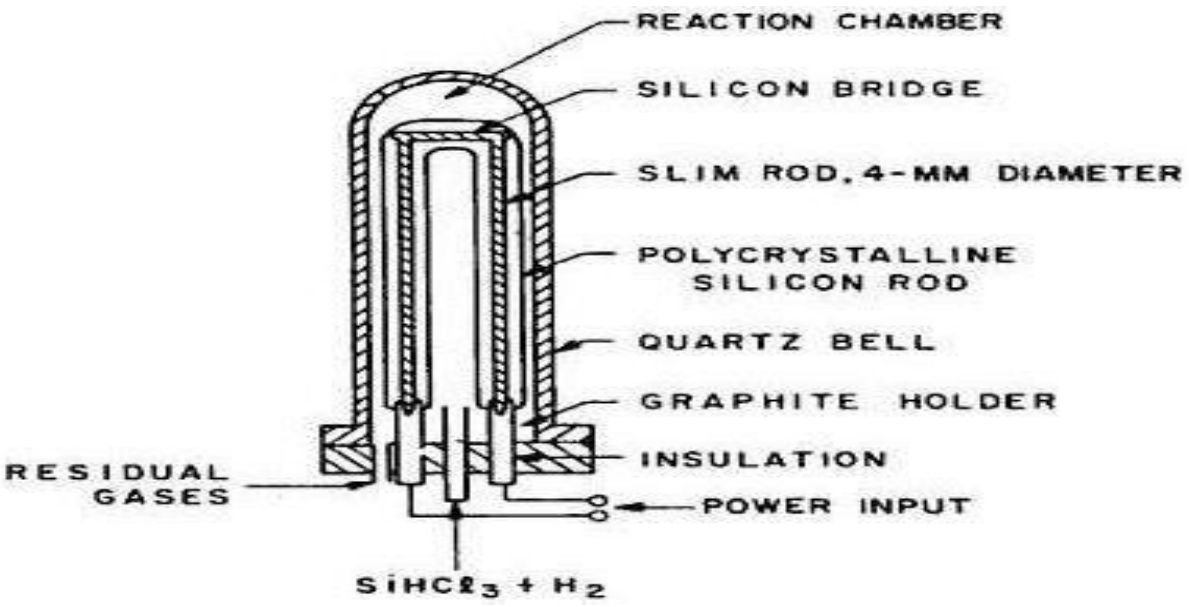
The MGS after being drawn off, has to be solidified at a purity of 98%. But this purity is not enough for the manufacture of semiconductor devices. So, the MGS has to be pulverized mechanically and reacted with anhydrous hydrogen chloride (HCI) to form trichlorosilane (SiHCI3). The reaction is shown below.

**Si + 3HCl = SiHCI3 + H2**




With the help of a catalyst, the reaction takes place at a nominal temperature of 300°C. The reaction creates products like silicon tetrachloride (SiCl4) and the chlorides of impurities. At this point the purification process occurs. The purification process has to be done by fractional distillation method as the products trichlorosilane and unwanted chlorides are liquids at room temperature.

The purified SiHCI3 is subjected to **chemical vapor deposition (CVD**). The chemical reaction is a hydrogen reduction of SiHCl3




**Schematic of a CVD reactor used for EGS production**

The chemical reaction is shown below.

**2SiHCl3 + 2H2 = 2Si + 6HCl**

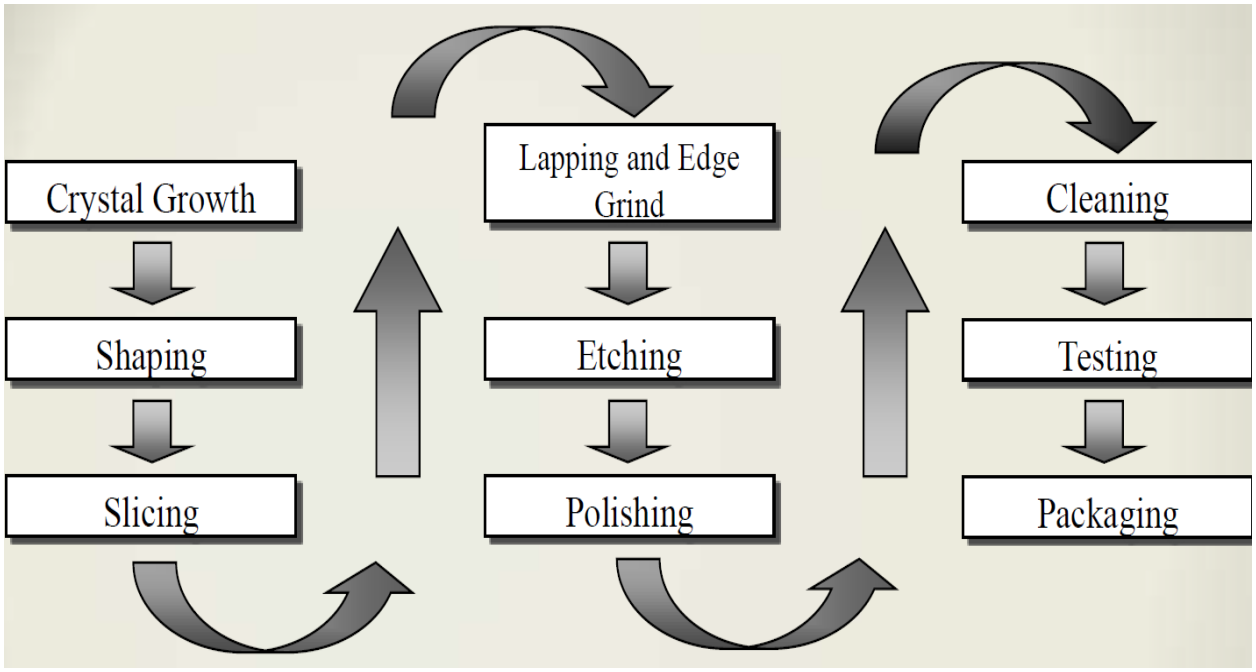
The reaction takes place in a CVD reactor. A resistance heated Si-rod (4-mm diameter), called a slim-rod, is used as the nucleation point for the deposition of silicon. Through the process rods of EGC are obtained which are up to 0.2 meters (or more) in diameter and several meters in length. EGS can be cut from these rods as single chunks or crushed into nuggets. In order to achieve high overall efficiency, a feedback or recycling of reaction of by-products is done. This is also shown in the figure above. EGS can also be produced by pyrolysis method in which silane (SiH4) will be reacted with heat. The reaction takes place at a high temperature of 900°C. The main advantage of using silane instead of trichlorosilane is the lower production cost and less production of harmful reaction by-products.

**SiH4 + HEAT = Si + 2H2**

In this process the CVD reactor is operated at about 900°C and supplied with silane instead of trichlorosilane. The advantages of producing EGS from silane are lower cost and less harmful reaction by-products.

**Q 8** Discuss different operations involved in preparation of wafers using schematic diagram. AKTU-2020-21

**Ans. WAFER PREPARATION**

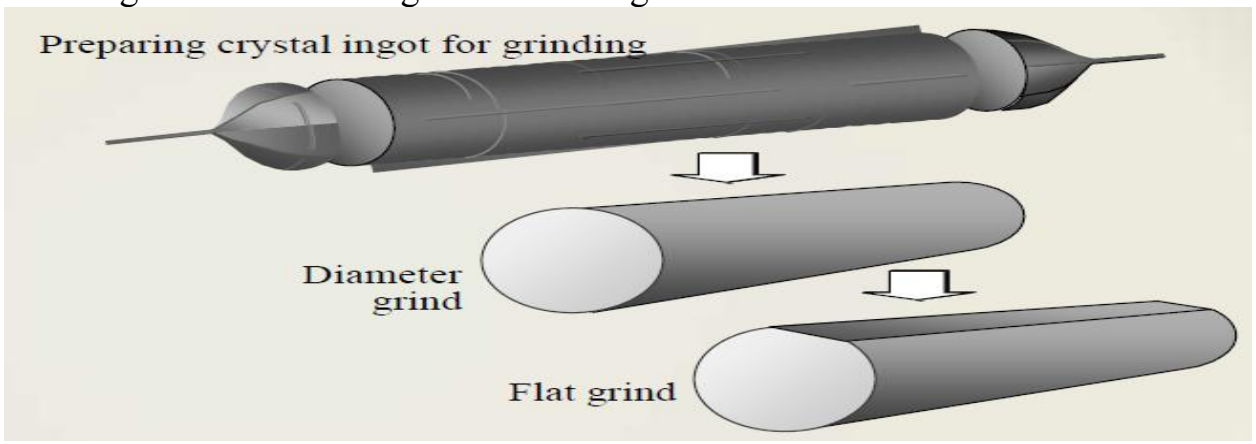



Shaping

The silicon crystal obtained after Cz process is called "ingot".

• The first shaping operation removes the seed and tang ends from the ingot.

• The ingot surface is then grounded throughout to an exact diameter.




Wafer Slicing

• Once the ingot surface is made smooth, ingot is sliced in wafers by high speed "diamond saw".

• Slicing is done by inner diameter sawing using a diamond saw.

• It is rotated at a high speed and then moved across the ingot to obtain wafer slices.

• Slicing is done very slowly.
• Thicker wafers are usually preferred.

Lapping & Edge Grind

• After slicing there is a variation in the thickness of the sliced wafer. So, it can't be used directly for IC fabrication.
• The wafers a mechanically lapped on both the sides.
• Lapping is done in order to remove the cracked or damaged surface of the wafer.
• After lapping edge grinding takes place.

Lapping Machine

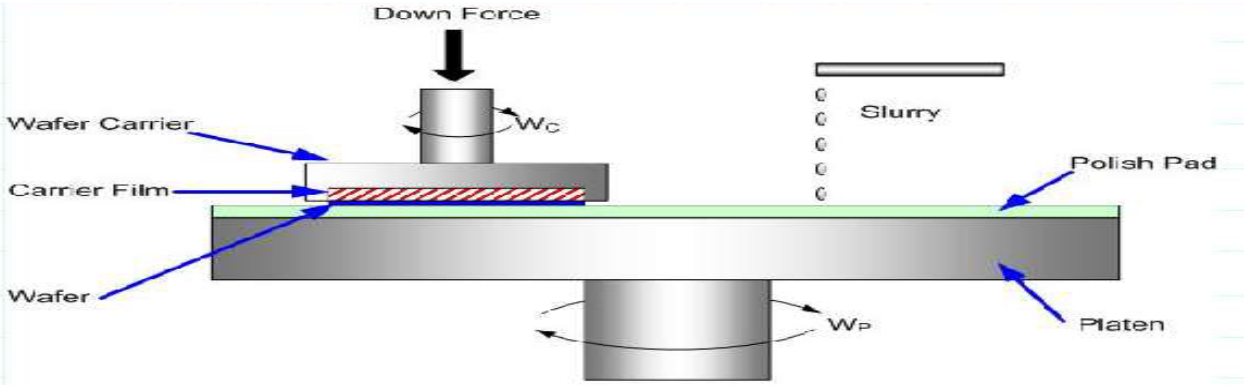
Etching

Etching is the process of selectively removing unwanted semiconductor material from the wafer.

• Wet etching: chemical solution is used.
• Dry Etching: sputtering method is used.
• Chemical etching removes the remaining damaged and contaminated regions of the wafer.
• A mixture of HF & $HNO_3$, is used for chemical etching.

Wafer Polishing

• The purpose of polishing is to provide smooth surface of the wafer.
• The wafer surface is polished to mirror like finish.




Cleaning

Wafers are cleaned and dried for use in IC fabrication.

• The final wafer thickness is about one third of the sliced wafer.

Testing

• Wafer testing is a step performed during semiconductor device fabrication.

• During this step, performed before a wafer is sent to die preparation.

• All individual integrated circuits that are present on the wafer are tested for functional defects.

• The wafer testing is performed by a piece of test equipment called a wafer prober.

Packaging

- Packaging is done in order to protect the wafers from moisture & contaminants.
- The completed packages are inspected, sealed, and marked with a special ink to indicate product type, date, package code, and speed**.**

**Q 9.** Explain various processing consideration while design wafer. AKTU-2022-23

**Ans. PROCESSING CONSIDERATIONS**

In the IC processing of silicon wafers it is usually necessary to maintain the purity and perfection of the material.

**1.Gettering Treatments**

- Conductive impurity precipitates, which act like shorts between the emitter and collector. Metallic impurities, such as transition group elements, are responsible for these effects. These elements are located at interstitial or substitutional lattice sites and are generation recombination centers for carriers. The precipitated forms of these impurities are usually silicides, which are electrically conductive.
- To remove impurities from devices, a variety of processing techniques are available, termed "gettering" treatments.

- "Gettering" is a general term taken to mean a process that removes harmful impurities or defects from the regions in a wafer where devices are fabricated.
- Among these techniques are ways to pretreat (i.e., pregetter) silicon wafers prior to IC processing.

**1st Technique Gettering Treatments**

- Technique of removing impurities involves intentionally damaging the back surface of the wafer. Mechanical abrasion methods such as lapping or sand blasting have been used for this purpose.
- This technique involves using a Q-pulsed, Nd:YAG laser.
- The laser beam is rastered along the back surface to create an array of micromachined spots. Depending on the energy density and proximity of the spots, the silicon lattice is damaged and/or strained by the high-energy pulse. Upon thermal processing, dislocations emanate from the spots. If the stresses placed on the wafer during furnace processing are low, the dislocations remain localized on the back surface. The dislocations represent favorable trapping sites for fast diffusing

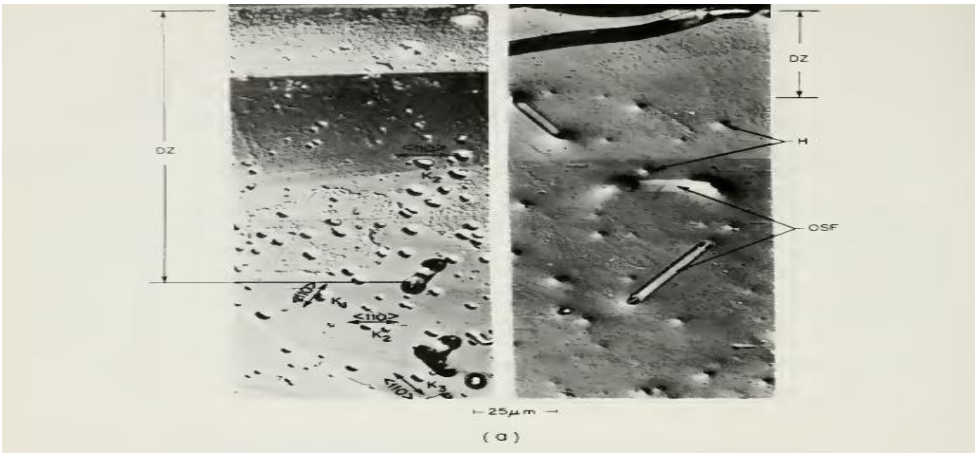



Fig. 32 (a) The left-hand photograph shows a denuded zone (DZ) in a wafer cross section after a preferential etch. $K_1$, $K_2$, and $K_3$ are small stacking fault defects. The right-hand photograph is another wafer cross section showing stacking faults (OSF) and precipitate features (H) below the DZ. *(Courtesy G. A. Rozgonyi.)*

(Fig. 1).

**2ND Technique Gettering Treatments**

This methods uses the defects associated with oxygen precipitation for trapping sites. These methods use one or more thermal cycles to produce the desired result." They usually involve a high-temperature cycle (over 1050°C in nitrogen), which removes oxygen from the surface of the wafer by evaporation. This lowers the oxygen content near the surface so that precipitation does not occur, because the supersaturated condition has been removed. The depth of the oxygen-poor region

is a function of time and temperature, and depends on the diffusivity of oxygen in silcon (Fig. 1). The region represents a defect-free zone (denuded zone) for device fabrication. Additional thermal cycles can be added to promote the formation o precipitates and defects in the interior of the wafer. This approach is called "intrinsic gettering" because the oxygen is native to the wafer. Intrinsic gettering is attractive because it fills the volume of the wafer with trapping site.

**2.Thermal Stress Factors**

We generally want to maintain the crtystal perfection of wafers through the device fabrication process, and to keep them mechanically under formed. Wafers are typically processed in furnaces using racks with a high wafer-diameter-to-spacing ratio. Upon removing the wafer from a high-temperature furnace, the wafer edges cool rapidly by radiation to the surroundings, but the wafer centers remain relatively hotter.' The resultant temperature gradient creates a thermal stress S that can be estimated as:

$$S = aE\,dT$$

where a is the coefficient of thermal expansion, E is Young's modulus, and dT the temperature difference across the slice. If these stresses exceed the yield strength (the maximum stress the material will accommodate without irreversible deformation) of the material, dislocations will form. Stresses are usually kept to acceptable levels by slowly withdrawing wafers from the furnace to minimize the temperature gradient, or by lowering the furnace temperature'^ prior to removing the wafers to the point where the yield strength at the removal temperature exceeds the stresses imposed.

**Q10.** Explain importance of wafer cleaning technology? Explain its type? AKTU2022-23

OR

Demonstrate RCA cleaning with analysis of all steps and chemicals.AKTU2021-22

**Ans. WAFER CLEANING**

Wafer cleaning process is the removal of chemical and particle impurities without altering ordamaging the wafer surface or substrate. The surface of the wafer must be maintained not affected so that roughness, corrosion or pitting negates the results of the wafer cleaning process.

Wafer Cleaning Step

**Pre-Diffusion Clean**-Creates a surface that is free from metallic, particulate and organic contaminants. In certain cases native oxide or chemical oxides need to be removed

**Metallic Ion Removal Clean**-Eliminate metallic ions which can have detrimental effect on device operation

Particle Removal Clean-Particle removal from surface using chemical or mechanical scrubbing using Megasonic cleaning.

**Post Etch Clean-**Remove photo resist and polymers left after etching process. Remove photo resist and solid residue including "etch polymer" Film Removal Clean-Silicon nitride etching/strip, Oxide etching/strip, Silicon etching and metal etching/strip

**WET WAFER CLEANING**

RCA(Radio Corporation of America) clean is a standard set of wafer cleaning steps which need to be performed before high-temperature processing steps (oxidation, diffusion, CVD) of silicon wafers in semiconductor manufacturing.

Werner Kern developed the basic procedure in 1965 while working for RCA, the Radio Corporation of America.

It involves the following chemical processes performed in sequence:

1. Removal of the organic contaminants (organic clean + particle clean)
2. Removal of thin oxide layer (oxide strip, optional)
3. Removal of ionic contamination (ionic clean)

Ideally, the steps below are carried out by immersing the wafers in solutions prepared in fused silica or fused quartz vessels (borosilicate glassware must not be used, as its impurities leach out and cause contamination.

**First step (SC-1): organic clean + particle clean**

The first step (called SC-1, where SC stands for Standard Clean) is performed with a solution of (ratios may vary)

- 5 parts of deionized water
- 1 part of ammonia water, (29% by weight of $NH_3$)
- 1 part of aqueous $H_2O_2$ (hydrogen peroxide, 30%)

at 75 or 80 °C typically for 10 minutes. This base-peroxide mixture removes organic residues. Particles are also very effectively removed, even insoluble particles, since SC-1 modifies the surface and particle zeta potentials and causes them to repel.This treatment results in the formation of a thin silicon dioxide layer (about 10 Angstrom) on the silicon surface, along with a certain degree of metallic contamination (notably iron) that will be removed in subsequent steps.

**Second step (optional): oxide strip**

The optional second step (for bare silicon wafers) is a short immersion in a 1:100 or 1:50 solution of aqueous HF (hydrofluoric acid) at 25 °C for about fifteen seconds, in order to remove the thin oxide layer and some fraction of ionic contaminants. If this step is performed without ultra high purity materials and ultra clean containers, it can lead to recontamination since the bare silicon surface is

very reactive. In any case, the subsequent step (SC-2) dissolves and regrows the oxide layer.[

**Third step (SC-2): ionic clean**

The third and last step (called SC-2) is performed with a solution of (ratios may vary)

- 6 parts of deionized water
- 1 part of aqueous HCl (hydrochloric acid, 37% by weight)
- 1 part of aqueous $H_2O_2$ (hydrogen peroxide, 30%)

at 75 or 80 °C, typically for 10 minutes. This treatment effectively removes the remaining traces of metallic (ionic) contaminants, some of which were introduced in the SC-1 cleaning step.[ It also leaves a thin passivizing layer on the wafer surface, which protects the surface from subsequent contamination (bare exposed silicon is contaminated immediately).

**Fourth step: rinsing and drying**

Provided the RCA clean is performed with high-purity chemicals and clean glassware, it results in a very clean wafer surface while the wafer is still submersed in water. The rinsing and drying steps must be performed correctly (e.g., with flowing water) since the surface can be easily recontaminated by organics and particulates floating on the surface of water. A variety of procedures can be used to rinse and dry the wafer effectively

**DRY CLEANING**

Ozone cleaning process offers two methods that can improve silicon wafer cleaning and reduce chemical use. The main part of the process uses ozone to convert organic residue on wafers into carbon dioxide through oxidation. The wafers coming out of this process have reduced levels of particle contamination when compared to traditional cleaning methods using chemical baths. The improved cleaning performance of the patented advanced ozone cleaning process can increase facility throughput and improve semiconductor quality while reducing chemical use

**Q11. Explain the terms: SSI, LSI, MSI and VLSI.** AKTU-2020-21

**Ans.**

**SSI: Small-scale Integration (Gates< 10)**

The first integrated circuits contained only a few transistors. Called "Small-Scale Integration"(SSI), Design products are flip flops & gates.

**MSl: Medium-scale Integration (10<Gates< 1000)**

The next step in the development of integrated circuits, taken in the late 1960s, Medium scale integration (MSI) has 10 to 100 gates/chip electronic components per chip. Design products are , registers & counters

**LSl: Large-scale Integration (Gates> 1000)**

Large scale integration (LSI)-100 to 10,000 gates/chip or electronic components per chip. The first microprocessor, calculator chips and RAMs of 1Kbit developed in the 1970s had below four thousand transistors.

**VLSI: Very Large-scale Integration (Gates>100000)**

The final step in the development process, starting in the 1980s.Very large scale integration (VLSI)-more than 10,000 gates/chip or electronic components per chip Design products are microprocessors & high capacity memories.

**Q12.** What are the advantages of Integrated circuits?

**Ans.** The major advantages of integrated circuits over those made by interconnecting discrete components are as follows:

1. small size
2. Low cost
3. Improved performance
4. High reliability and ruggedness
5. Low power consumption
6. Easy troubleshooting
7. Increased operating speed
8. Less weight ,volume
9. Easy replacement

**Q13.** How does analog ICs, differ from digital ICs?

**Ans. Analog Integrated Circuits**

Analog or Linear ICs can produce continuous output depending on the input signal. From the name of the IC we can deduce that the output is a linear function of the input signal. Op-amp (operational amplifier) is one of the types of linear ICs which are used in amplifiers, timers and counters, oscillators etc.

**Digital Integrated Circuits**

Unlike Analog ICs, Digital ICs never give a continuous output signal. Instead it operates only during defined states. Digital ICs are used mostly in microprocessor and various memory applications. Logic gates are the building blocks of Digital ICs which operate either at 0 or 1.

**Q14** Discuss the IC Based on the method or techniques used in manufacturing.

Based on the method or techniques used in manufacturing them, *types of ICs* can be divided into three classes:

1. Monolithic ICs
2. Thin and thick film ICs
3. Hybrid or multichip ICs

# UNIT-02

## Q 1. Explain the purpose of oxidation? AKTU-2021-22

**Ans. Purpose of oxidation**

1. Masking element against diffusion of dopants.
2. Gate oxide in MOS devices
3. Isolation between devices
4. Electrical isolation of multilevel metallization
5. Used as surface passivation

## Q2. Explain Plasma Oxidation technique for the growth of oxide layer? AKTU-2021-22

**Ans.** The anodic plasma-oxidation process offers the possibility of growing high-quality oxides at temperatures even lower than those achieved with the high-pressure technique. This process has all the advantages associated with low-temperature processing, such as movement of previous diffusions and suppression of defect formation. Anodic plasma oxidation can grow reasonably thick oxides (on the order of 1 μm) at low temperatures (<600°C) at growth rates up to about 1 μm/h. Plasma oxidation process offers the possibility of growing high quality oxides at temperature even lower than those achieved with the high pressure technique. It is low temperature vacuum process. The plasma is produced by high frequency discharge or a DC electron source. Place the wafer in a uniform density region of plasma. Biasing it positively below the plasma potential. Allow it to collect active charged oxygen species. The beneficial effect of plasma oxidation will occur with selective oxidationtechniques (where portions of the wafer are masked against oxidation). Appropriate oxidation masks include aluminum oxide, magnesium oxide, and silicon nitride patterned by the photolithographic technique. Oxide properties, specifically the etch rate, refractive index, stress, fixed charge, interface states, and breakdown strength of plasma oxides grown at 500°C compare favorably to the properties of thermal oxides grown at 1100°C.

**Q3.Explain Molecular Beam Epitaxy process in detail. Also write the advantages and disadvantages of this method? AKTU-2021-22,22-23,21-22**

**Ans. Molecular Beam Epitaxy (MBE) growth system**

Molecular Beam Epitaxy (MBE) is an advanced ultra-high-vacuum facility (basic pressure $10^{-13}$ bar) to make compound semiconductor materials with great precision (< 0.01 nanometer) and purity (>99.99999%). These materials are layered one on top of the other to form semiconductor devices such as transistors and lasers, which are devices being used in such applications as fiber-optics, cellular phones, satellites, radar systems, solar cells, and display devices.

It is physical evaporation process, with no chemical reactions involved in it. The epitaxial layer, which we will be grown on Si substrate is usually Si in

Silicon technology. The evaporation is done under very high vacuum condition. The heart of the MBE process is the ultra high vacuum pumping. After achieving the ultra high vacuum condition, next step is to evaporate the epitaxial species (Si). Silicon (Si) has very high melting point so it is very diffcult the silicon by thermal heating. So, evaporation process of silicon is done with electron gun. The electron beam is focused on the silicon source, after that silicon is evaporated. In MBE system, we have 2 pumps. The pumps are used to achieve the ultra high vacuum condition. Also we have a silicon source. We have crucible in which the silicon is placed. e - beam is focused on the silicon source. From this silicon source, silicon is evaporated from the conical shape. Effusion cell is used to introduce the dopants. Effusion cell is used to introduce the dopants. There is a small opening at the mouth of the effusion cell, through which evaporated dopants come out. We have two shutters, these are controlled by microcontroller The shutters are used to control the layer thickness and amont of dopants incorporated in the epitaxial layer. Sample holder supports the Silicon substrate. Additionally we have a heater and

thermocouple. Thermocouple is used to measure the temperature of the substrate Substrate temperature is usually kept 400 0 C to 800 0 C.

So, we have the **following steps for MBE**

- Create the ultra high vacuum condition with the help of pumps.
- Switch on the electron gun in order to evaporate the silicon.
- Heat the effusion cell in order to incorporate the dopant.
- Open the shutter at the top of two cones, dopants will be mixed with silicon.

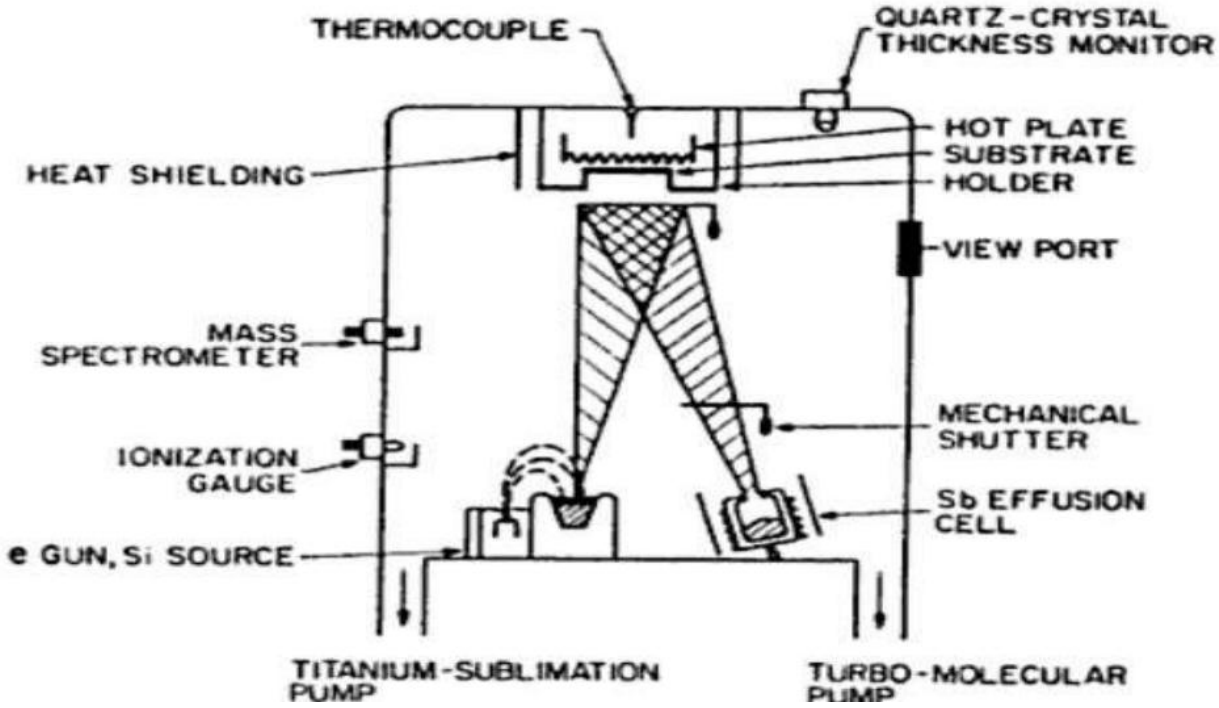



**Fig:** Molecular Beam Epitaxy (MBE) growth system

. **Advantages of MBE over VPE**

1. **Low Temperature Process:** because of low temperature process, the auto doping effect can be minimized from substrate to epitaxial layer.

2. **Precise Control of Doping:** this is because there is no chemical reaction involved. It is only physical evaporation process. Measured quantity of the dopants can be evaporated.
3. **Growth Rate:** growth rate can be achieved as small as possible.
4. **No Boundary (Stagnant) Layer Problem:** there is no boundary problem, so the growth rate is equal for all the substrate.

**Disadvantages of MBE over VPE**

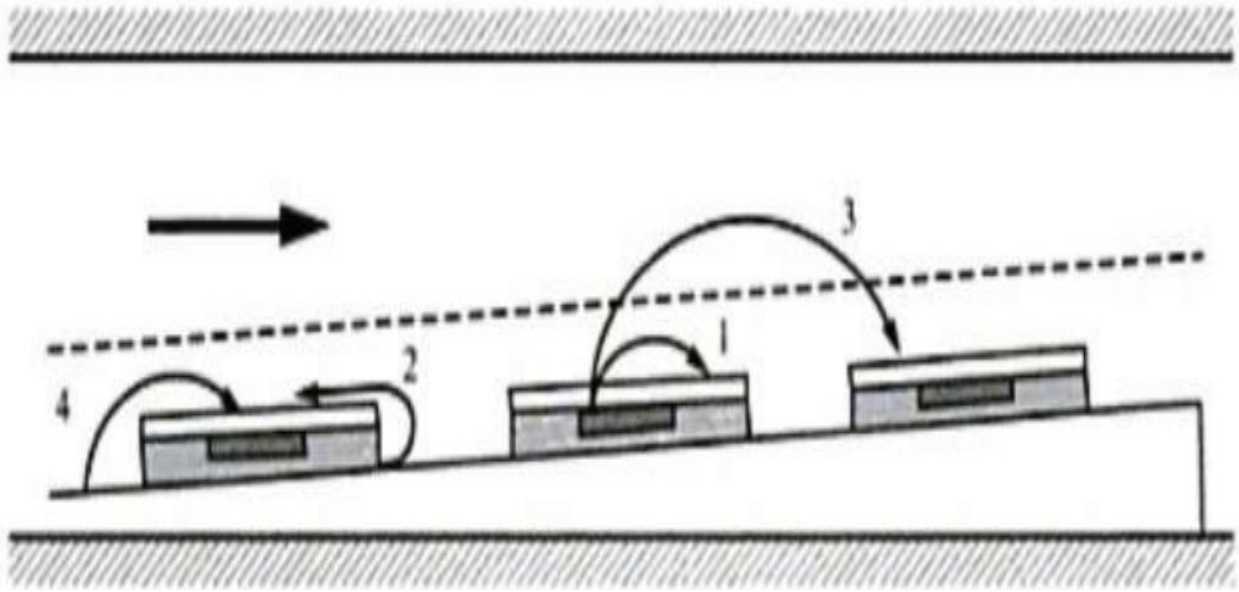
1. Very costly equipment
2. Very complicated equipment

**Q 4 . What is Epitaxy? AKTU-2022-23**

**Ans.** Epitaxy is the combination of 2 words, Epi – upon and Taxis – ordered. It is the process of growing a thin crystalline layer on acrystalline substrate. Epitaxial layer is always thinner than the substrate. There is no chemical reaction between epitaxial layer & substrate layer

**Q 5. What is auto doping? AKTU-2022-23**

**Ans.** It is the process of transporting doping atoms from the substrate into the epitaxial layer. So, in auto doping unintentional dopants are incorporated from the substrate. This effect is called **"auto doping"**.



1 – wafer front side 2- wafer back side 3 – other wafer 4 – susceptor

These unintended impurities may come to the wafer from:

- wafer front side
- wafer back side
- other wafer
- Susceptor

The auto doping can be removed by pre – epitaxial process inside the reactor. For this HCL etching takes place at 12000 C.

$$\mathbf{4HCl + Si \rightarrow SiCl_4 + 2H_2}$$

## Q 6. Explain with a diagram Vapor Phase Epitaxy?AKTU-2022-23

**Ans. Vapor Phase Epitaxy**

In VPE, the material which we want to grow on the Si substrate must be in vapor form. We use some gases & chemical reactants. Liquid with very high vapor pressure instead of gas may also be used. We have a graphite susceptor on which substrate (samples) are placed inside a reactor. Also, we have a flow of gas. The gas is containing the reactants. As the reactants flow over the samples, there will be deposition
at the top of the samples. This process is called "Vapor Phase Epitaxy". containing the reactants.

The material which we want to deposit is now on the samples. Samples are already present inside the reactor. The gas is flowing inside the reactor with a finite velocity. At the point of contact on the substrate, the velocity is zero. So, at other places the velocity of the gas is finite in the reactor. It means, inside the reactor the velocity of the gas at different regions is different. The velocity of the gas just right next to the first substrate is very low. It means reactants are not moving very fast. It means, we have a boundary layer. So for VPE the width of the boundary layer is very important.
The flow of gas inside the reactor is characterized by Reynolds number Re & is
given by:

$$R_e = \frac{D_r}{\mu} v\rho$$

$R_e$-Reynolds number
$D_r$-is Diameter through which the gas is moving
*V*- is velocity of the gas flow.
$\rho$-is the density of the gas
μ -is the viscosity of the gas

**Reaction chemistry of Epitaxy**

Basically there are 4 Silicon sources used for epitaxial growth.

a) $SiCl_4$ – Silicon tetrachloride
b) $SiHCl_3$ –Trichlorosilane
c) $SiH2Cl_2$ – Dichlorosilane
d) $SiH_4$ – Silane

Out of these four, SiCl4 is most widely used for industrial use. So, the overall reaction is the hydrogen reduction of the Silicon tetrachloride gas.

During the epitaxial growth the Cl/H ratio remains constant because neither Cl nor H is incorporated into the epitaxial layer. The epitaxial layer is growing it means, there is deposition of reactants (Si) from the gases on the surface of the substrate. The deposition rate is always –ve. The deposition rate is –ve; it means the concentration of the reactants outside the reactor is larger than that of at the reactor. i.e., NG>NS. It means reactants are moving from higher concentration region to lower concentration region. So, epitaxial process takes place because of –ve

## Q 7.Calculate the oxidation time required for the thermal oxidation of 100 A and 5000 A thickness at 1000 0C. Note B = 5.2x105 A2/min and B/A = 111 A/min.. AKTU-2022-23

**Ans.** To calculate the oxidation time required for the thermal oxidation of silicon wafers with thicknesses of 100 Ångströms (A) and 5000 Ångströms (A) at 1000 °C, you can use the Deal-Grove model for silicon oxidation. The Deal-Grove model describes the oxidation rate of silicon as follows:

$$R = \frac{B}{A} \exp \frac{-E_a}{kT} - \exp \frac{-E_a}{kT}$$

Where:

- R is the oxidation rate (in Ångströms per minute, A/min).
- B is the process-dependent constant, which is given as 5.2×1055.2×105 A²/min.
- A is the initial thickness of silicon.
- Ea is the activation energy for silicon oxidation, which is approximately 1.2 eV.
- kis the Boltzmann constant, approximately 8.6173×10−58.6173×10−5 eV/K.
- T is the absolute temperature in Kelvin, which is 1000 °C + 273.15 = 1273.15 K.

Given that B/A=111 A/min, we can now calculate the oxidation rate RR for both 100 Ångströms and 5000 Ångströms thick silicon wafers.

.

For 100 Ångströms thick wafer:
R100=111 A/min
For 5000 Ångströms thick wafer:
R5000=111×exp(−1.2 eV8.6173×10−5 eV/K×1273.15 K) A/min

Now, you can calculate the oxidation time (tt) for each thickness using the formula:

$$t = A/R$$

For 100 Ångströms thick wafer:

$$t_{100} = \frac{100\ \text{A}}{111\ \text{A/min}}$$

For 5000 Ångströms thick wafer:

$$t_{5000} = \frac{5000\ \text{A}}{R_{5000}}$$

Now, calculate $t_{100}$ and $t_{5000}$:

$$t_{100} = \frac{100\ \text{A}}{111\ \text{A/min}} \approx 0.9009\ \text{min}$$

$$t_{5000} = \frac{5000\ \text{A}}{R_{5000}} \approx 22.3\ \text{min}$$

So, the oxidation time required for a 100 Ångströms thick wafer at 1000 °C is approximately 0.9009 minutes, and for a 5000 Ångströms thick wafer, it is approximately 22.3 minutes.

**Q 8. What is meant by annealing?. AKTU-2022-23**

**Ans.** Annealing refers to a series of heat treatment processes that are used to modify the properties of semiconductor materials, typically silicon, and other related materials used in the manufacturing of electronic devices**.**

## Q9 Explain the different types of deposition reactors used for VPE.? AKTU2020-21

**Ans. TYPE OF REACTORS USED IN EPITAXIAL PROCESS**

Basically we are having 3 reactors for epitaxial growth

- Horizontal reactor
- Vertical reactor
- Barrel reactor

In horizontal reactor, we have are having inclined sample holder as shown in fig. In this kind of reactor, we have parallel gas flow.

In vertical reactor, gas flow is the normal to the surface of the sample. In vertical reactor, we can't place much more samples at a time.For mass production, the barrel reactor is used.

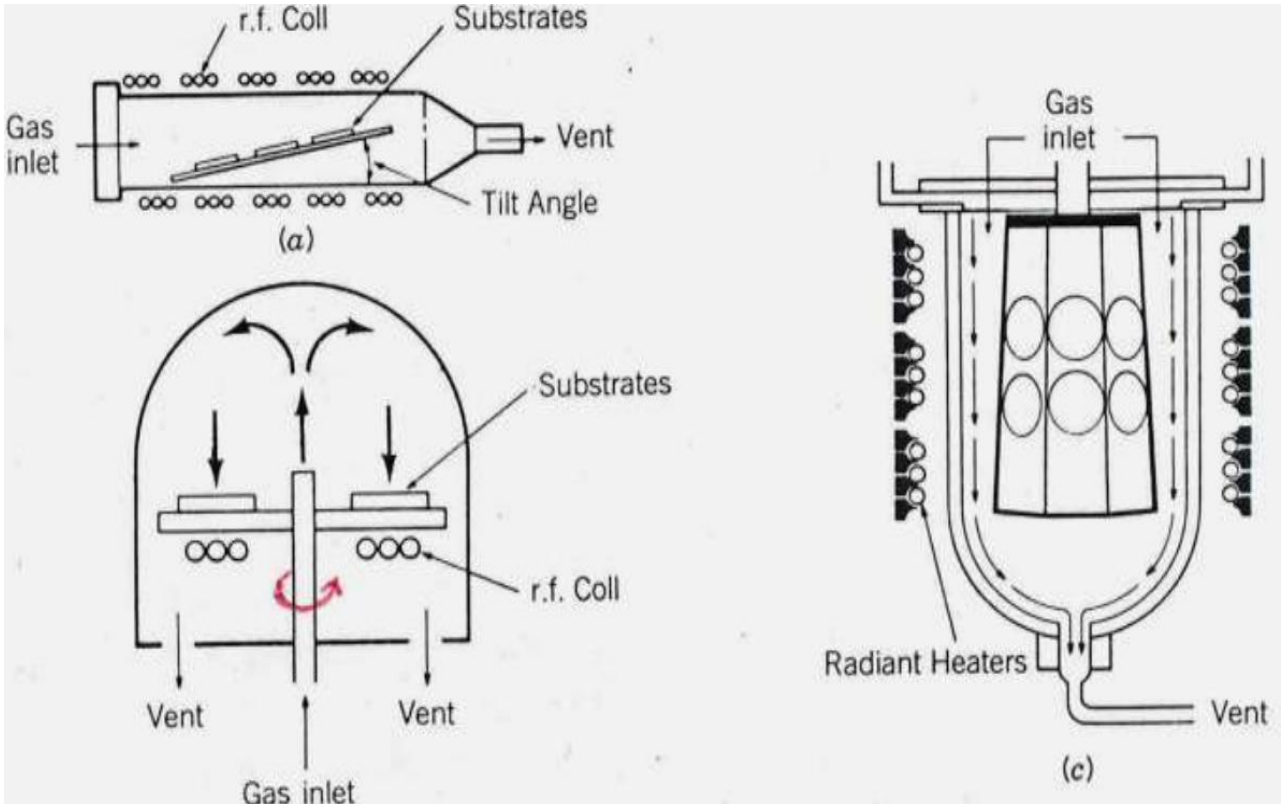


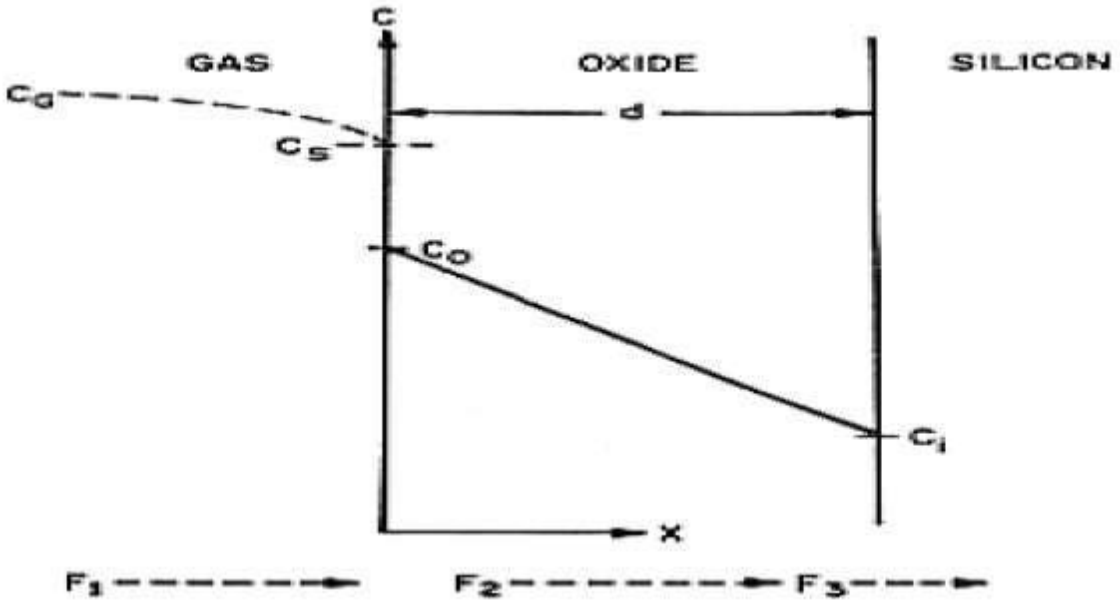

**Fig: epitaxial reactors (a) horizontal (b) vertical (c) barrel**

In this kind of reactor, the reactor the sample holder is a barrel or drum. In this barrel, we are having small grooves. In each of the grooves, the samples are placed. The barrel can be rotate for uniform epitaxial growth. The flow of the gas is parallel to the surface of the wafer. In a barrel reactor, lot of samples can be placed in a same time. Better growth can be achieved by rotating the barrel. For the epitaxial reactor, there are lot of steps. First step is to filled up the reactor with hydrogen gas. Initially this hydrogen gas will clean the reactor. So the hydrogen gas will react with the air & will form water. After that heating of the reactor is required through RF heaters. This will the water in vaporized form. After that the vaporized water can be taken out from the gas outlet.

Next step is to filled up the reactor with the silicon sources. Growth process starts at a rate of 0.2 μm/min to 2.o μm/min. When the epitaxial growth has completed, we need to shut off the power. Remove the silicon sources & dopants. Dopants may be n type or p type. Reactor is cooled upto the ambient temperature. Since the reactor may consist of some gases, so we need to filled up the reactor with some inert gases. Usually the inert gas may be nitrogen, so that the reactor may be opened safely.

## Q10. Explain the chemistry and kinetics of growth using Deal& Grove's Model.. AKTU-2020-21

**Ans.** The Linear and Parabolic growth laws were developed by Deal and Grove, and are Known as the Linear Parabolic Model. This oxide growth model has been empirically proven to be accurate over a wide range of temperatures (700-1300°C), oxide thicknesses (300- 20,000 angstroms), and oxidant partial pressures (0.2-25 atmospheres). Fig.1 and 2 pictures various diffusions possible and the concentration of species during thermal oxidation and is the basis for Deal a Grov model.


C
GAS
OXIDE
SILICON
$C_G$
$C_S$
d
$C_O$
$C_i$
X
$F_1$
$F_2$
$F_3$

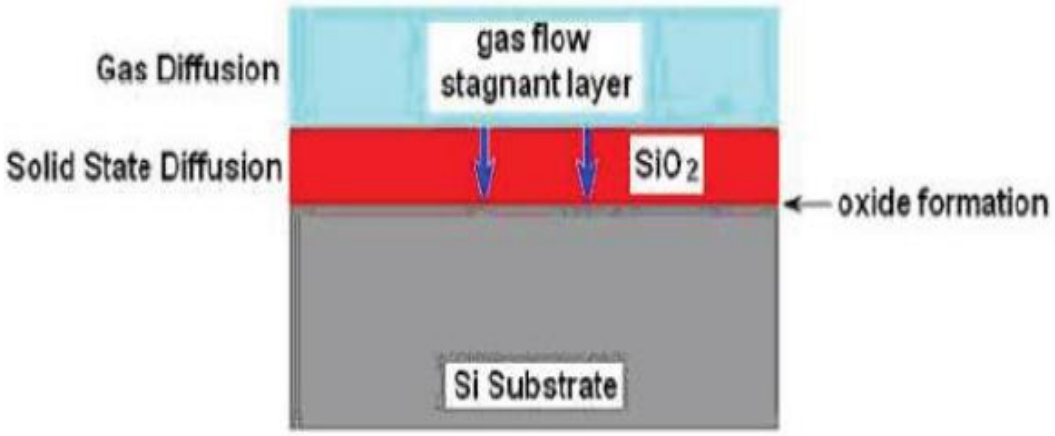



Fig. 1: A Model for thermal oxidation of silicon indicating various diffusions possible

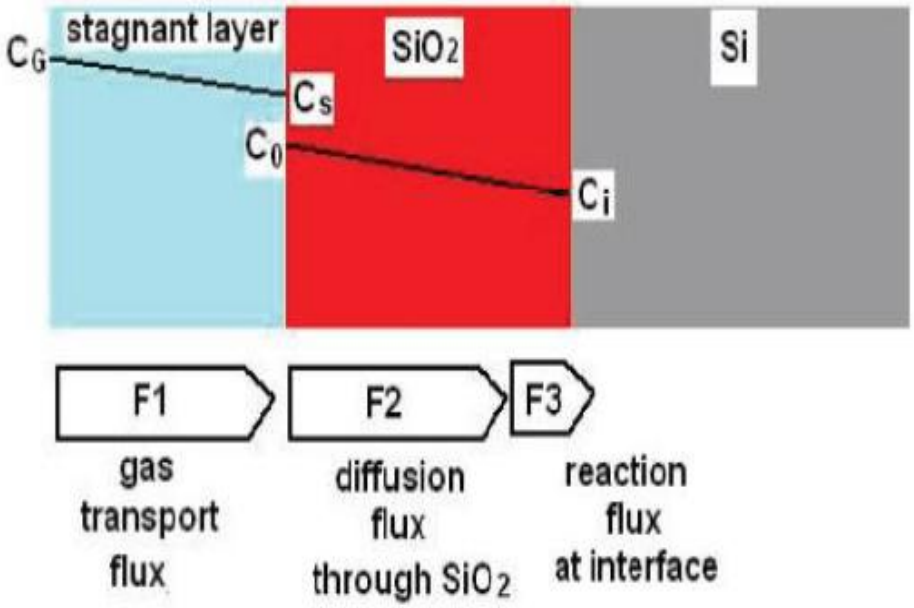



Fig.2: A Model for thermal oxidation of silicon indicating the concentration of species

Consider the Groove model for thermal oxidation of the silicon. Initially $SiO_2$ layer is not present. We have oxidizing species in the gas. Once the oxidizing species has reached the gas-oxide interface, it must diffuse through the existing oxide layer in order to reach the Si-$SiO_2$ interface. Once these oxidizing species reach the Si-$SiO_2$ interface, it must react with silicon.

• We have three fluxes F1, F2 & F3. Flux is the number of molecules or atoms crossing an unit area in an unit time.

• $C_G$ is the concentration of the oxidizing species in the gas.

• $C_S$ is the concentration of the oxidizing species next to the gas oxide interface.
• $C_0$ is the concentration at outer surface of the oxide.
• $C_i$ is the concentration at inner surface of the oxide.
• C* is the equilibrium concentration of the oxidizing species in the oxide layer.
• Where,
  - $F_1 = h_G (C_G - C_S)$
  - $F_1$ = flux of the oxidizing species in the gas.
  - $h_G$= gas phase mass transfer coefficient.
  - $C_G = P_G/kT$
  - $C_S = P_S/kT$

• According to Henry's Law "the concentration of a species within a solid is proportional to the partial pressure of that species in the surrounding gas".

- So,
  - ✓ $C^* = HP_G$
  - ✓ $C^0 = HP_S$
- Where,
  - ✓ $P_G$= Partial pressure of the oxidizing species in the gas.
  - ✓ $P_S$ = Partial pressure of the oxidizing species right next to gas-oxide interface.
  - ✓ H= Henry's Coefficient

- So,

$$F_1 = h(C^* - C_0);\ h = \frac{h_G}{HkT} \text{ ---------- } -(1)$$

- ✓ $$F_2 = \frac{D}{x}(C_0 - C_i) \text{ ---------- } -(2)$$

$$F_3 = K_S C_i \text{ ---------- } -(3)$$

- $x$ is oxide thickness, Ks is reaction rate coefficient & D is diffusion constant.
- Under steady state conditions, these three fluxes must be equal.

- Equating (2) & (3), we get
  - ✓ $C_i = \frac{C_0}{1+K_s\frac{x}{D}}$ ----------(4)
  - ✓ Put $C_i$ in eq (3)
  - ✓ $F_3 = K_s \frac{C_0}{1+K_s\frac{x}{D}}$ ----------(5)
  - ✓ Now equating eq. (1) & (5)

- Now, consider the following cases,

✓ **Case 1:** $D \to 0;\ C_0 \to C* \ \&\ Ci \to 0$

- Physical significance is that diffusion is controlling the oxidation.

✓ **Case 2:** $D \to \infty;\ C_0 \to \frac{C*}{1+\frac{Ks}{h}}\ \&\ Ci \to \frac{C*}{1+\frac{Ks}{h}}$

- Physical significance is that reaction rate is controlling the oxidation.

✓ $C_0 = \frac{C*\left(1+\frac{K_S x}{D}\right)}{1+\frac{K_S}{h}+\frac{K_S x}{D}}$ ----------(6)

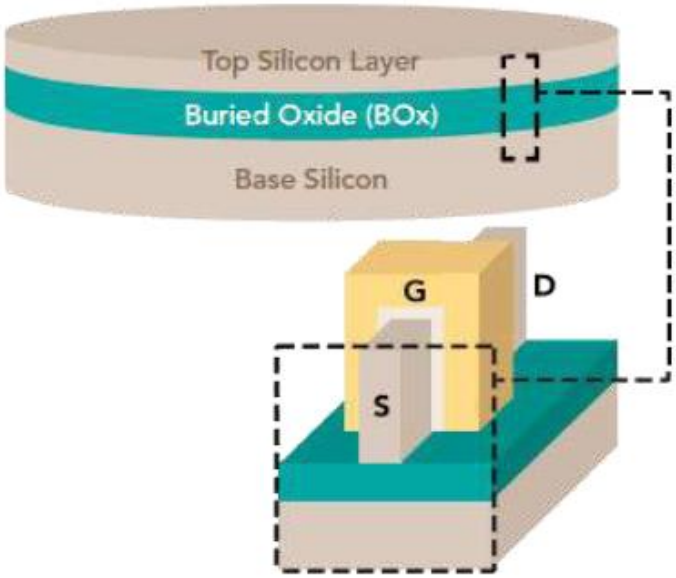
- Put eq. (6) in eq. (4), we get

✓ $C_i = \frac{C*}{1+\frac{K_S}{h}+\frac{K_S x}{D}}$ ----------(7)

**Q11.What is Silicon On Insulators(SOI) technology**?

**Ans.** Silicon-On-Insulator (SOI) wafers, transistors are formed in thin layers of silicon that are isolated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide. The silicon layer thickness ranges from several microns for electrical power switching devices to less than 500 Å for high-performance microprocessors.

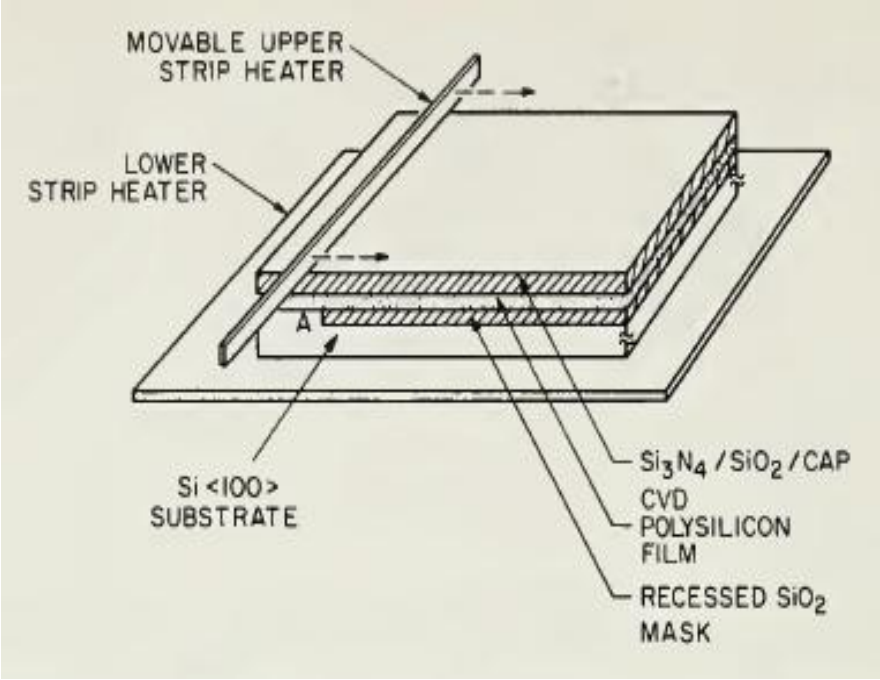
Isolating the active transistor from the rest of the silicon substrate reduces the electrical current leakage that would otherwise degrade the performance of the transistor. Since the area of electrically active silicon is limited to the immediate region around the transistor, switching speeds are increased and sensitivity to "soft errors", a major concern for large-scale data storage and high-volume servers, is greatly reduced




Silicon on insulator (SOI) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon in semiconductor Manufacturing.Silicon-On-Insulator (SOI) is a new way of starting the chip making process, by replacing the bulk silicon wafers (approximately 0.75 mm thick) with wafers which have three layers; a thin surface layer of silicon (from a few hundred Angstrom to several microns thick) where the transistors are formed, an underlying layer of insulating material and a support or "handle" silicon wafer. The insulating layer, usually made of silicon dioxide and referred to as the "buried oxide" or "BOX", is usually a few thousand Angstroms thick.

**Q12. Explain Silicon on Amorphous Substrates?**

**Ans .**Silicon on insulator (SOI) is a recent nonepitaxial approach to providing single-crystal silicon. With this technology, amorphous or polycrystalline silicon is recrystallized on an amorphous substrate. Figure shows a setup for recrystallization using a strip heater. The process is considered nonepitaxial as this silicon film is not single crystal as-deposited. Energy for the process can also be supplied by electron beam or laser**.**




Substrates can be conventional silicon wafers covered with silicon nitride or silicon dioxide or even fused quartz substrates. This substrate is then coated with polysilicon in a low-pressure CVD process to a thickness of 0.5 μm. A movable strip heater (Fig.), positioned above one of the openings to the substrate, melts the polysilicon through to the substrate.The heater is then moved laterally, and, with the substrate acting as a seed, single-crystal silicon is grown laterally over the oxide-covered regions. The thermal stability of the molten zone is improved if it is capped with oxide and nitride layers. Capping also prevents contamination of the film. This technique is suitable for recrystallizing large areas, such as an entire wafer. Similar procedures using a scanned CW argon laser have been reported.

**Q13.What is homoepitaxy?**

**Ans.** In Homo Epitaxy Same material is grown on the substrate. Doping concentration & resistivity may be different.

- Ex: Si on Si.

**Q14.Compare wet oxidation with dry oxidation. State the purpose of oxidation?**

**Ans. Purpose of oxidation**

1.Masking element against diffusion of dopants.
2. Gate oxide in MOS devices
3. Isolation between devices
4. Electrical isolation of multilevel metallization
5. Used as surface passivation

**1. Dry Oxidation**

$O_2$ & HCl are used to grow oxide layer.

• It is also known as HCl dry oxidation.
• It has lower growth rate than wet oxidation.
• HCl is used to improve the electrical characteristics of the oxide layer.
• It has excellent dielectric properties.
• During the oxidation Cl is concentrated on the Si-$SiO_2$ interface.
• Cl increases the life of the oxide layer.

The oxide layer formed by HCl dry oxidation is used as gate oxide in MOS devices.

• This oxide layer has very stable threshold voltage property.
• Reaction involved:

$$4HCl + O_2 \longrightarrow 2H_2O + 2Cl_2$$

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

**2. Wet Oxidation**

• Also known as pyrogenic (producing heat) wet oxidation.
• Pure $H_2$ & $O_2$ are directly supplied to the furnace.
• Vaporized $H_2O$ is obtained by increasing the $H_2$ & $O_2$ in the furnace.
• The oxide layer is grown by vaporized $H_2O$.
• Advantage of wet oxidation is that, it can employ various partial pressures of $H_2O$.

$$2H_2 + O_2 \rightarrow 2H_2O$$
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

**Q15.Compare Homo & Hetero Epitaxy. State the Applications of Epitaxial Growth.**
**Ans.**

| Homo Epitaxy | Hetero Epitaxy |
|---|---|
| Same material is grown onthe substrate | Different material is grownin the substrate. |
| Doping concentration & resistivitymay be different. | Doping concentration &resistivity may/may not bedifferent. |
| Ex: Si on Si | Ex: GaAs on Si |

**Applications of Epitaxial Growth**

- Nanotechnology
- Semiconductor fabrication
- High quality crystal growth(silicon –germanium, gallium-nitride)
- To grow layers of pre-doped silicon (in pacemakers, vending machine)
- To deposit organic molecules onto crystalline substrate

# UNIT-03

**Q 1. What are PR materials? AKTU-2022-23**

**Ans.** Photosensitive compound used in microelectronics is called photoresist. There are 2 kind of photoresist, -ve and +ve. Photoresist actually have 2 materials in it polymer and photosensitive compound. The photosensitive compound get activated when it is exposed to UV. radiation. After getting activate it absorbs energy. The energy is
transferred to the polymer molecules.

**Q2. Name photo masking technique commonly used. AKTU-2022-23**

**Ans.** Integrated circuit (IC) fabrication, a commonly used photo masking technique is called (Optical Lithography) "photolithography" or simply "lithography." Photolithography is a crucial step in the semiconductor manufacturing process, used to create intricate patterns on semiconductor wafers.

**Q3. What are positive and negative photoresist?** ? **AKTU-2021-22.**

**Ans. Let us consider –ve photoresist.**
When the polymer molecules get energy from activated photosensitive compound,the molecular width of the polymer molecules increases. So, when the width of the polymer molecules increases, it becomes more difficult to dissolve in any developer solution. The regions which are not exposed to light, there is no absorption of energy. So, the width of the polymer molecules will not increase.The regions not exposed can be removed by developer solution. Negative resist are CODAC MICRONEG 747 • The +ve resist have opposite manner. Positive resist are HPR 206,MP2400

**Q 4 . What are the disadvantages of Electron Beam Lithography? AKTU-2022-23**

**Ans. Problems associated with e – beam Lithography**

**1. Slowness**: Since, e – beam lithography offers direct writing the e – beam scan all over the surface of the substrate. If we use +ve e – beam resist, it has to be exposed to e –beam radiation to considerable amount of time.

**2. Low Throughput**: as every wafer need a longer time to process the radiation, so larger number of wafer can't be processed during a given time.
**3. Proximity effect**: as the e beam has high energy, so it may scatter the regular wafer atoms. It is proximity effect.

**Q 5.Differentiate between positive and negative photoresist.AKTU-2022-23**

**Ans.** we have two substrate, one with –veresist and other with +ve resist. Let we have exposed these two resist in UV rays. Now, we have to dissolve the softened resist using developer solution (solvent).

**The +ve resist will dissolve early as compared to –ve resist.**

First, the resist will absorb the developer solution. Consider the case of –ve resist, the absorption of the developer solution will cause swelling of resist • So, the feature size will change. Therefore minimum feature size will get slightly distorted. **So, -ve resist offers poor resolution, i.e., +ve resist are better.**

**Q6.Briefly explain Electron Beam Lithography? List its importanceAKTU-2022-23**

**Ans. E – Beam Lithography**

Process of transferring geometrical pattern from a mask to the Si Substrate.. In this process, first of all coating the Si Substrate is done, with photoresist. First step is to coat the Substrate with photoresist. Photoresist is the radiation sensitive polymer.When the photoresist is exposed to E – Beam its properties changes.So, in lithography process, 1 or 2 drops of photoresist are used.Put these drops in Si Substrate. Spi the Substrate very quickly. Hold the substrate in vacuum chuck. Spin it very fast (4000 rpm). Now, we have thin uniform coating of the photoresist film on the wafer. By, varying the spin rate thickness of the coating layer (photoresist) can be adjusted. Second step is to expose it to UV radiation.This exposure may/may not be through a mask. Mask is a glass plate with opaque and transparent patterns on it.Mask has opaque and transparent patterns. Now allow the radiation to fall on it. As, the photoresist is radiation sensitive material, so only regions, which are exposed to the radiation, their properties will change. The expose regions get soften

(+ve photoresist). Third step is developing the substrate.This substrate is now soaked in a developing solution. Fourth step is Etching. Photoresist can be removed by photoresist removal solution. Now the exposed oxide can be etched away.

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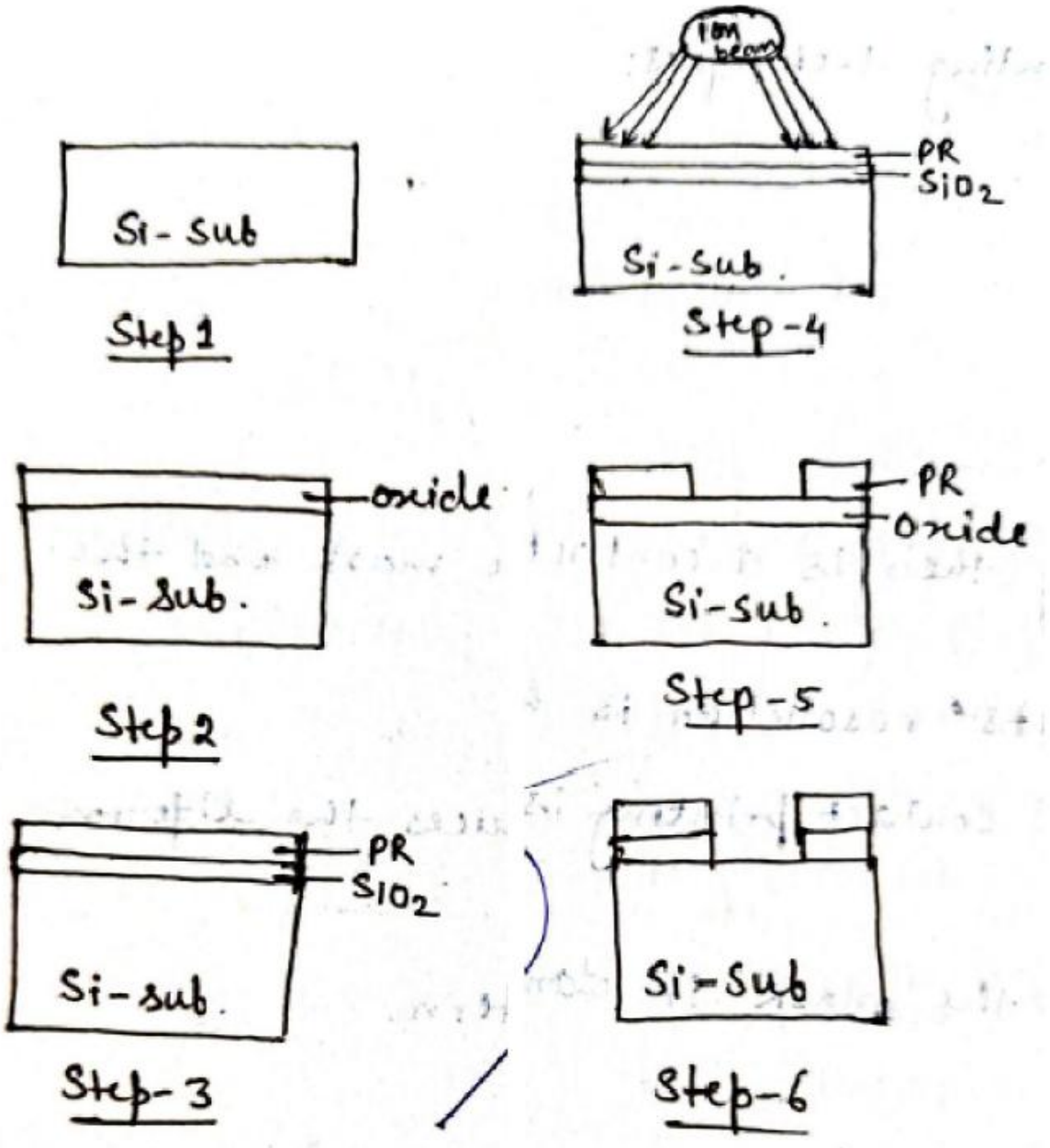



Electron beam (diameter 0.2 μm to 0.5 μm) is used instead of E – Beam. In this kind of lithography, no need of mask, i.e., direct writing is possible. It has greater depth of focus.The scan system is computer controlled. The e

beam can be switch on or off as per requirement. The movement of the e – beam taking place on very small region called “scan field”. The resolution of e – beam lithography will be very good, if the beam diameter is small. So, for good resolution we should have very good focused e – beam.

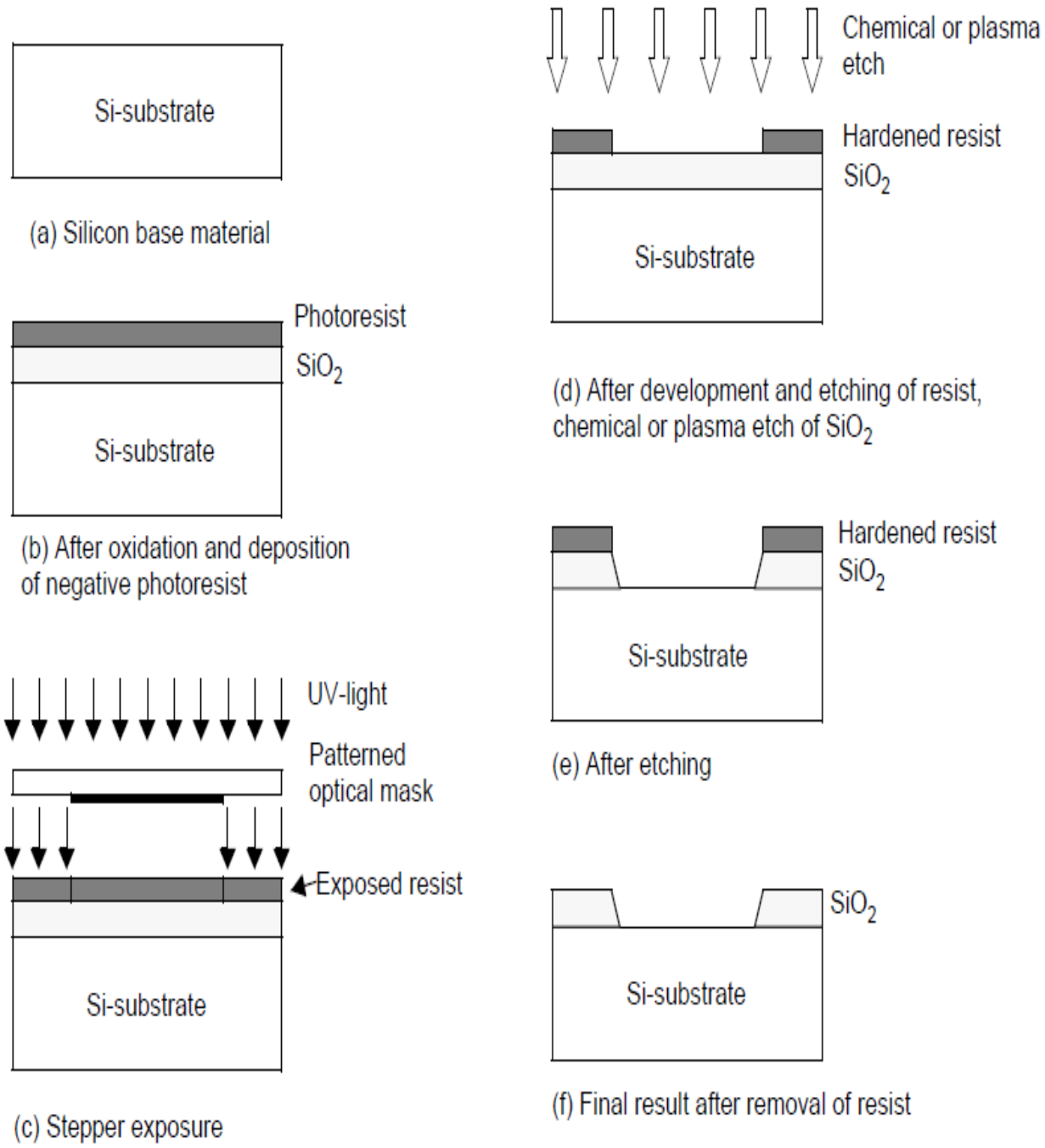
Problems associated with e – beam Lithography 1. Slowness: Since, e – beam lithography offers direct writing the e –beam scan all over the surface of the substrate. If we use +ve e – beam resist, it has to be exposed to e –beam radiation to considerable amount of time. 2. Low Throughput: as every wafer need a longer time to process the radiation, so larger number of wafer can’t beprocessed during a given time. 3. Proximity effect: as the e beam has high energy, so it may scatter the regular wafer atoms. It is proximity effect

**Q 7 List all process steps of pattern transfer with diagram.. AKTU-2022-23 ,20-21**

**Ans. Process of transferring geometrical pattern from a mask to the Si Substrate.**

• In this process, first of all coating the Si Substrate is done, with photoresist.
• First step is to coat the Substrate with photoresist.
• Photoresist is the radiation sensitive polymer.
• When the photoresist is exposed to UV light its properties changes.
• So, in lithography process, 1 or 2 drops of photoresist are used.
• Put these drops in Si Substrate.
• Spin the Substrate very quickly.
• Hold the substrate in vacuum chuck.
• Spin it very fast (4000 rpm).
• Now, we have thin uniform coating of the photoresist film on the wafer.
By, varying the spin rate thickness of the coating layer (photoresist) can be adjusted.
• Second step is to expose it to UV radiation.
• This exposure may/may not be through a mask.
• Mask is a glass plate with opaque and transparent patterns on it.
• Mask has opaque and transparent patterns.
• Now allow the radiation to fall on it.

• As, the photoresist is radiation sensitive material, so only regions, which are exposed to the radiation, their properties will change.
• The exposed regions get soften (+ve photoresist).
• Third step is developing the substrate.
• This substrate is now soaked in a developing solution.
• Fourth step is Etching.
• Photoresist can be removed by photoresist removal solution.
• Now the exposed oxide can be etched away.




**Q8 Explain the process of polysilicon film deposition. ? AKTU2020-21**

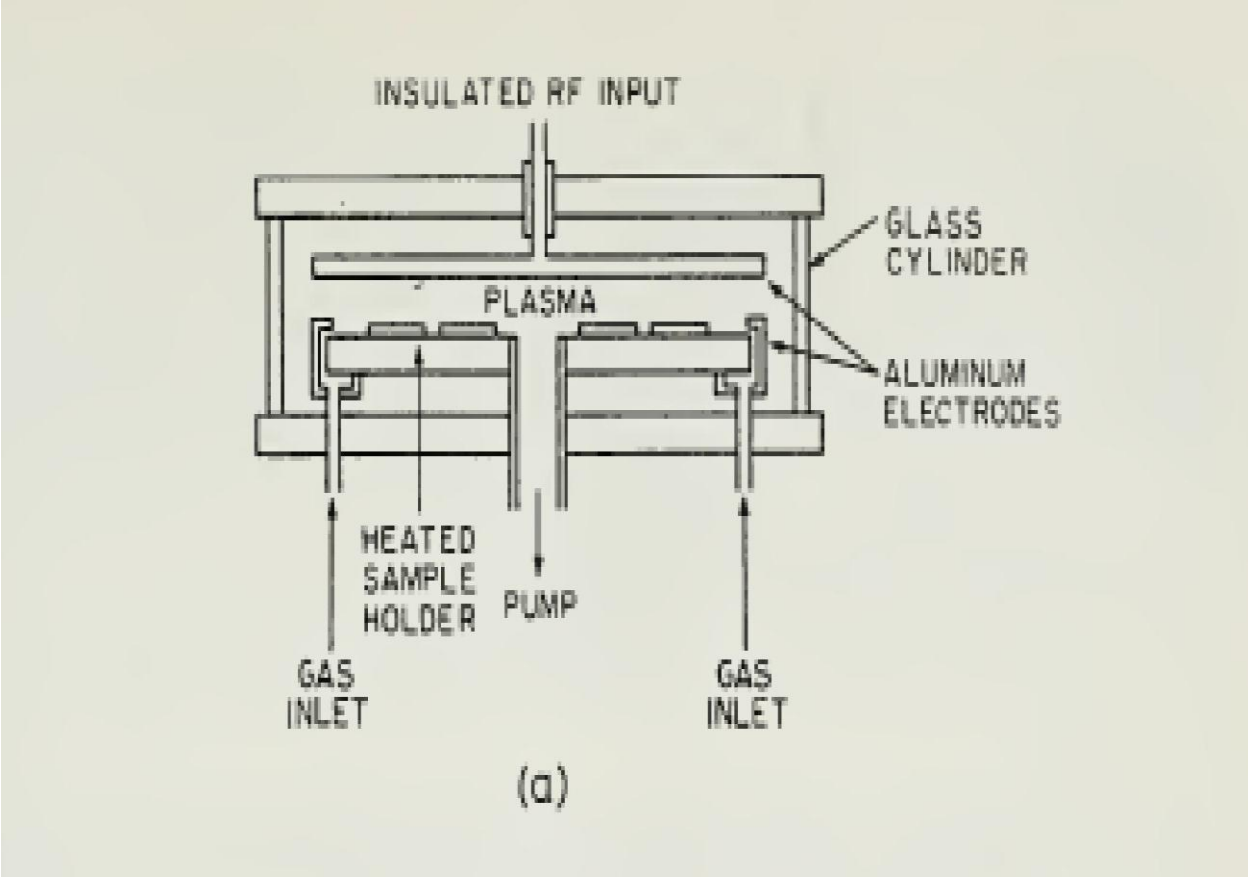
**Ans. Polysilicon**

Polysilicon is used as the gate electrode in MOS devices. It is also used

for highvalue resistors, diffusion sources to form shallow junctions, conductors, and to ensure ohmic contact to crystalline silicon. The polysilicon is deposited by pyrolyzing silane between 600 and 650°C in a low-pressure reactor (Fig. a)

**SiH4 (g) >Si (s) + 2H2 (gas)**

Either pure silane or 20 to 30% silane in nitrogen is bled into the LPCVD system at a pressure of 0.2 to 1.0 torr. The properties of the LPCVD polysilicon films are determined by the deposition pressure, silane concentration, deposition temperature, and dopant content.




Amorphous silicon can be prepared by the glow discharge decomposition of silane. Processing parameters such as deposition rate are affected by deposition variables such as the total pressure, reactant partial pressure, discharge frequency and power, electrode materials, gas species, reactor geometry, pumping speed, electrode spacing, and deposition temperature The

higher the deposition temperature and RF power, the higher is the deposition rate. Polysilicon can be doped by adding phosphine, arsine, or diborane to the reactants (in-situ doping). Polysilicon can be oxidized in dry oxygen at temperatures between 900oC and 1000oC to form an insulator between the doped polysilicon gate and other conducting layers. The resulting material, semi-insulating polysilicon (SIPOS) is also employed as a passivating coating for high voltage devices.

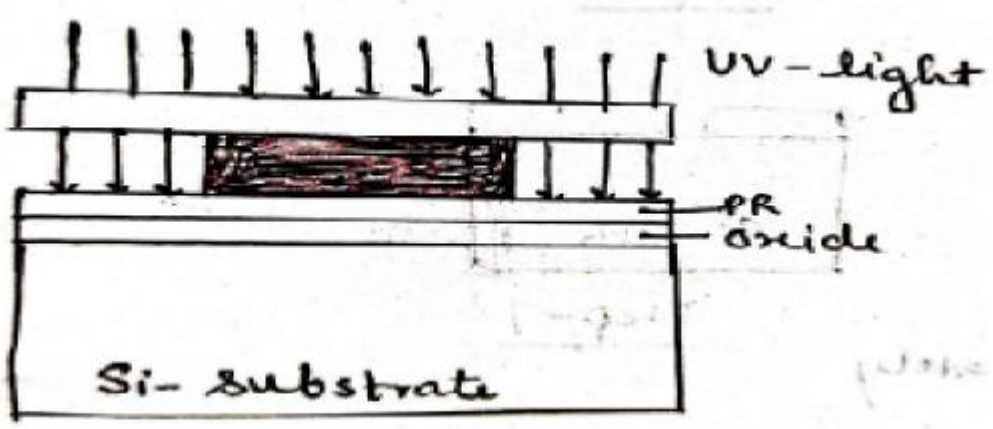
**Q9. Describe the process of optical lithography. Classify optical lithography based on placement of wafer and mask.AKTU-2020-21**

**Ans.** Process of transferring geometrical pattern from a mask to the Si Substrate.. In this process, first of all coating the Si Substrate is done, with photoresist. First step is to coat the Substrate with photoresist. Photoresist is the radiation sensitive polymer.When the photoresist is exposed to UV light its properties changes.

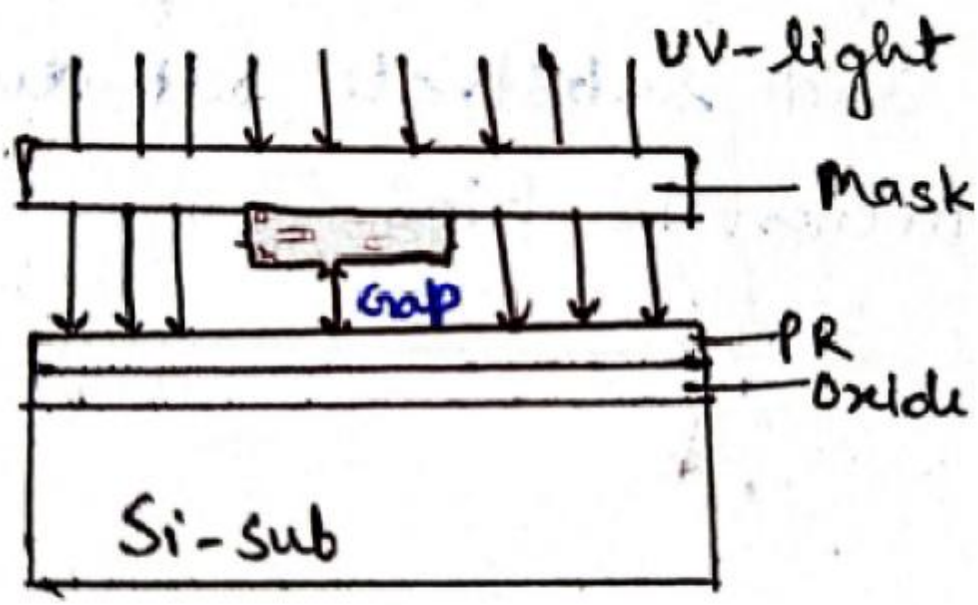
OPTICAL LITHOGRAPHY It can be classified in 3 categories.

1. Contact printing
2. Proximity printing
3. Projection printing

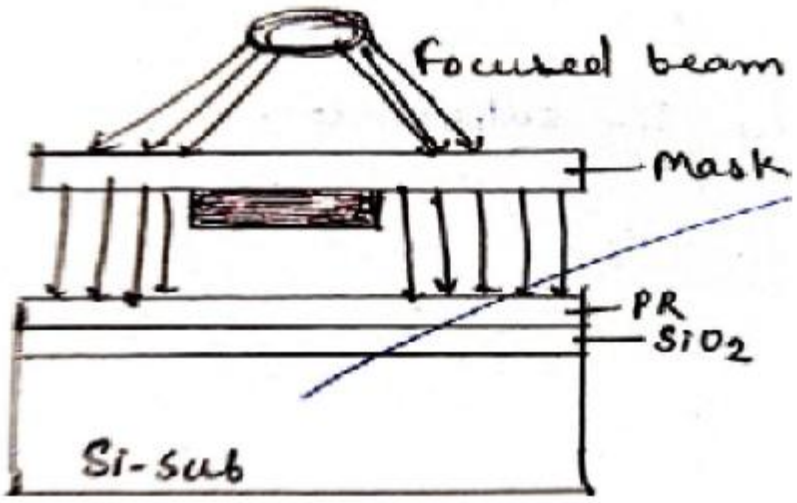
**1. Contact Printing** : In contact printing, the wafer is in the contact with the mask. There is no gap between the mask and the wafer, so the resolution will be high.The disadvantage of contact printing is that the life of the mask is reduced. Also, if there is some dirt on the mask, it can damage pattern on the mask. this printing technique, the photo mask pressed against the resist coated wafer with a pressure typically in the range of 0.05 atm to 0.3 atm and exposure by light of wavelength near 400 micro meters.




**2. Proximity Printing**: In proximity printing, the wafer and mask have some gap between them.The life of mask is somewhat larger than contact printing.But the resolution is smaller than that for contact printing. In proximity or shadow printing, there exists a gap between mask and wafer in the range of 20 to 50 micro meters. Typically, the resolution of proximity printing is 2 to 4 micro meter and is therefore not suitable for a process requiring less than a 2 um minimum line width.



**3. Projection Printing :** In projection printing, the mask is not in the contact with the wafer .Here the image of the mask is focused on the wafer. So, there is no problem of life reduction of the mask. Because of the highly focused image on the wafer, the resolution is high. A complicated optical setup is required in order to project the image of the mask on the wafer.




**Q10. What is wet chemical etching? Explain how etching reaction take place by using HNA. Mention the purpose of each acid in it.**? **AKTU-2020-21**

**Ans.**

**Wet Etching**

• Some chemical solution is used for wet etching.

• There are some chemical reactions involved, so it is also called "wet chemical etching".

• For wet etching, put the substrate into etchant solution.

• There are following steps**.**

• **First step** is to transport of Etchant.

• The etchants are in the solution.

• Let the sample is immersed in the etchant solution.

• The layer of the etchant solution adjacent to SiO2 layer will react immediately.
• Let HF is the etchant solution.
• So, in order to etching process to keep in progress, fresh supply of etchant solution is required.
• **Second step** is surface reaction.
• SiO2 layer reacts with etchant.
• **Third step** is transport of reaction products.
• After etching reaction, products can be removed.
• Most commonly used etchant is HNA for Silicon.
• HNA is Hydro Fluoric Nitric acid Aqua (or Acetic Acid).

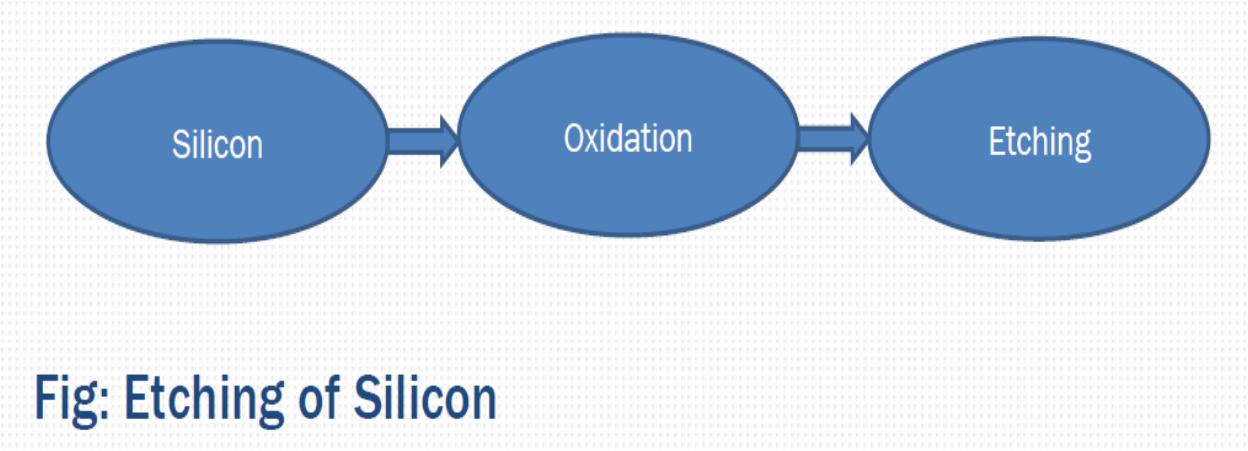
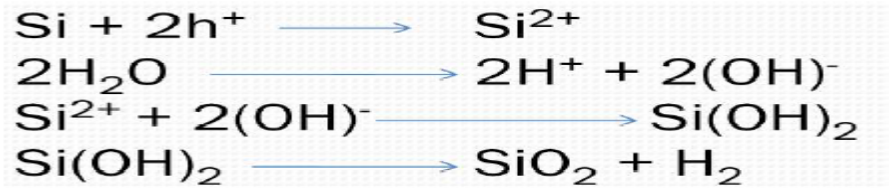



Fig: Etching of Silicon

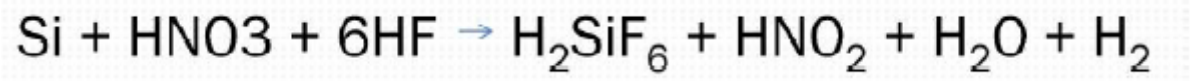
It is difficult process.It is done basically in 2 steps. First step is to convert Si into SiO2. Second step is to etch the SiO2.So, it means that etchants (HNA) have more than one component. One for oxidizing the silicon & other for etch that oxidized silicon.
• In order to etching of silicon, HNO3 (Nitric Acid) gives 2 holes. Small amount of HNO2 reacts with HNO3.

$$HNO_2 + HNO_3 \rightarrow N_2O_4 + H_2O$$
$$N_2O_4 \rightarrow 2NO_2$$
$$2NO_2 \rightarrow 2NO_2^- + 2h^+$$

So, the purpose of HNO3 is to give 2 holes to react with Si to form SiO2 from Si2+.
**Oxidation of Silicon takes place as**




This is basic anodic oxidation. Now, this SiO2, can be etched away In etchant HNA, the purpose of HNO3 is to oxidize silicon to form SiO2.The purpose of HF is to dissolve the SiO2, which gives H2SiF6 and water, i.e.




**Q11. Explain Figure of merits of Lithography?**

**Ans Figure of merits of Lithography**

Figure of merits determines how good or bad the lithography process is
There are 3 figure of merits of lithography process.

1. Resolution
2. Throughput
3. Depth of focus

**Resolution** means what is the minimum feature size. It also means the precision at which the minimum feature size is achieved.

**Throughput** means how many wafers can be processed in a given time.

**Depth of Focus** determines the depth of penetration of the light in the resist.

**Q12. State the purpose of Polysilicon.?**

**Ans.** Purpose of Polysilicon

(1)Gate electrode material in MOS devices
(2)Conducting materials for multilevel metallization
(3)Contact materials for devices with shallow junctions.

**Q13. Briefly explain Ion – Beam Lithography?**

**Ans. Ion – Beam Lithography**

Ions are used instead of electrons, as in e – beam lithography. Since, ions havevery low energy as compared to electrons, so scattering problem is low. So, the ion beam lithography is usually preferred. For ion beam lithography, RF ion source is used. Ions may be, H+, He+ or Ar+ in the 100 keV of energy. RF ion source is a very big system, so it is prone to vibration.

**Q14. What is PHOTOMASK?**

**Ans.**

A photomask is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. They are commonly used in photolithography and the production of integrated circuits (ICs or "chips") in particular. Masks are used to produce a pattern on a substrate, normally a thin slice of silicon known as a wafer in the case of chip manufacturing. Lithographic photomasks are typically transparent fused silica blanks covered with a pattern defined with a chrome metal absorbing film. Photomasks are used at wavelengths of 365 nm, 248 nm, and 193 nm. Photomasks have also been developed for other forms of radiation such as 157 nm, 13.5 nm (EUV), Xray, electrons, and ions; but these require entirely new materials for the substrate and the pattern film.

**Q15. What is Etching?**

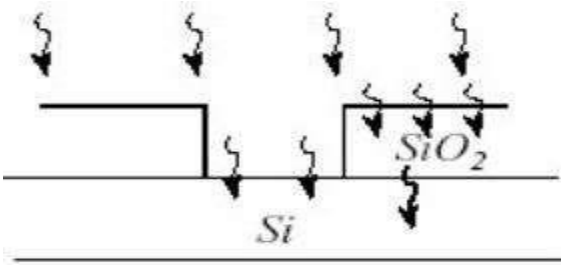
**Ans.**

It is the next step after lithography. It is the process by which the material can be uniformly removed from the wafer surface. In Lithography, pattern from the mask are transferred onto the wafer. After the Lithography, selected regions from the wafer can be etched away. The etching is usually done by dilute HF acid.

# UNIT-04

**Q1. What are the basic mechanisms of diffusion? AKTU-2021-22**

**Ans.** Diffusion is the process by which molecules move from an area of higher concentration to an area of lower concentration The diffusion process begins with the deposition of a shallow high concentration of the desired impurity in the Si surface through windows etched in the protective barrier layer.




**Q2. State Fick's second law of diffusion. AKTU-2021-22**

**Ans.**

## FICK'S SECOND LAW OF DIFFUSION

- Fick's second law of diffusion is given as:

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2}$$

Where, C = concentration of solute.
D = diffusivity
x = coordinate axis in the direction of solute flow
t = diffusion time

**Q3. What is diffusion furnace importance? AKTU-2022-23**

**Ans.**

A diffusion furnace is a specialized piece of equipment used in the semiconductor manufacturing process, particularly in the fabrication of integrated circuits. Its importance lies in its role in the diffusion process, a critical step in creating the desired electrical properties within semiconductor materials. The method impurity delivery to wafer is determined by the nature

of impurity source; Two-step diffusion is widely technique. Using this technique, the impurity concentration and profiles can be carefully controlled.

**Q 4 . What type of gaseous source commonly used in diffusion? AKTU-2022-23**

**Ans. Gaseous source commonly used in diffusion**

Boron Diffusion using $B_2H_6$ (Diborane) Gaseous Source, Nitrogen ($N_2$), Hydrogen (H2), Oxygen (O2)

**Q5. Demonstrate various diffusion profiles of dopant atom with appropriate equations and curves and compare them..AKTU-2021-22**

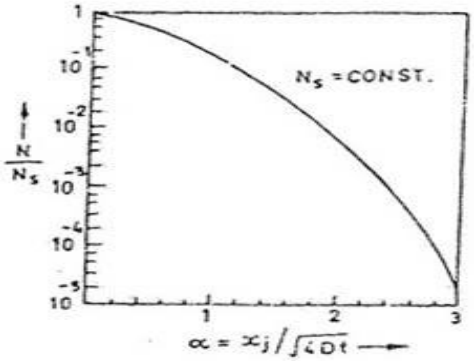
**Ans.** Depending on boundary equations the Ficks Law has two types of solutions. These solutions provide two types of impurity distribution namely constant source distribution following complimentary error function (erfc) and limited source distribution following Gaussian distribution function.

**1. Constant Source (erfc) Distribution**

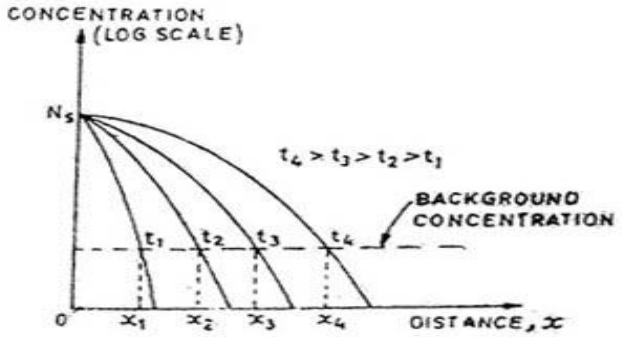
In this impurity distribution, the impurity concentration at the semiconductor surface is maintained at a constant level throughout the diffusion cycle. That is, $C(o,t) = CS = \text{Constant}$

The solution to the diffusion equation which is applicable in this situation is most easily obtained by first considering diffusion inside a material in which the initial concentration changes in same plane as x=0, from CS to 0. Thus the equation can be written as

$C(o,t) = CS = \text{Constant}$ and $C(x,t) = 0$




Complementary error function distribution.




Constant source diffusion profiles for various periods of time

Shown above is a graph of the complementary error function for a range of values of its argument. The change in concentration of impurities with time, as described by the equation is also shown in the figure above. The surface concentration is always held at CS, falling to some lower value away from the surface. If a sufficiently long time is allowed to elapse, it is possible for the entire slice to acquire a dopant level of CS per m3.

If the diffused impurity type is different from the resistivity type of the substrate material, a junction is formed at the points where the diffused impurity concentration is equal to the background concentration already present in the substrate.

In the fabrication of monolithic IC's, constant source diffusion is commonly used for the isolation and the emitter diffusion because it maintains a high surface concentration by a continuous introduction of dopant.

There is an upper limit to the concentration of any impurity that can be accommodated at the semiconductor wafer at some temperature. This maximum concentration which determines the surface concentration in constant source diffusion is called the solid solubility of the impurity.

**2. Limited Source Diffusion or Gaussian Diffusion**

Here a predetermined amount of impurity is introduced into the crystal unlike constant source diffusion. The diffusion takes place in two steps.

1. Predeposition Step – In this step a fixed number of impurity atoms are deposited on the silicon wafer during s short time.

2. Drive-in step – Here the impurity source is turned off and the amounts of impurities already deposited during the first step are allowed to diffuse into silicon water.

The essential difference between the two types of diffusion techniques is that the surface concentration is held constant for error function diffusion. It decays with time for the Gaussian type owing to a fixed available doping concentration Q

**Q6. Derive the diffusion equation. How the depth of diffusion is controlled during diffusion process? Give the solution of Fick's Law?.AKTU-2022-23**

**Ans.** Based on analogy between material transfer in a solution and heat transfer by conduction.

$$J = -D\frac{\partial C(x,t)}{\partial x}$$

**J=**rate of transfer of solute per unit area or diffusion flux

**C=**concentration of solute (function of x and t only)

**x=**coordinate axis in the direction of solute flow

**t=**diffusion time

**D=**diffusivity (Diffusion constant)

## FICK'S SECOND LAW OF DIFFUSION

- Law of conservation of matter: change in solute concentration per unit time= local decrease in diffusion flux in the absence of source.

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial J}{\partial x}(x,t)$$

- Combining with Fick's first law,

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial C(x,t)}{\partial x}\right]$$

- At low concentration of solute, diffusivity at a particular temperature can be considered a constant

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2}$$

Now, regarding the control of the depth of diffusion during the diffusion process, the key parameter is the diffusion time ($t$). The depth of diffusion ($\delta$) is related to the diffusion time and the diffusion coefficient ($D$) by the equation:

$\delta = \sqrt{4Dt}$

This equation shows that the depth of diffusion is directly proportional to the square root of the diffusion time and the diffusion coefficient. Therefore, controlling the diffusion time and adjusting the diffusion coefficient can be used to control the depth of diffusion.

As for the solution to Fick's Law, the general solution to the one-dimensional diffusion equation is given by:

$C(x,t) = C0(1 - \delta/x)$

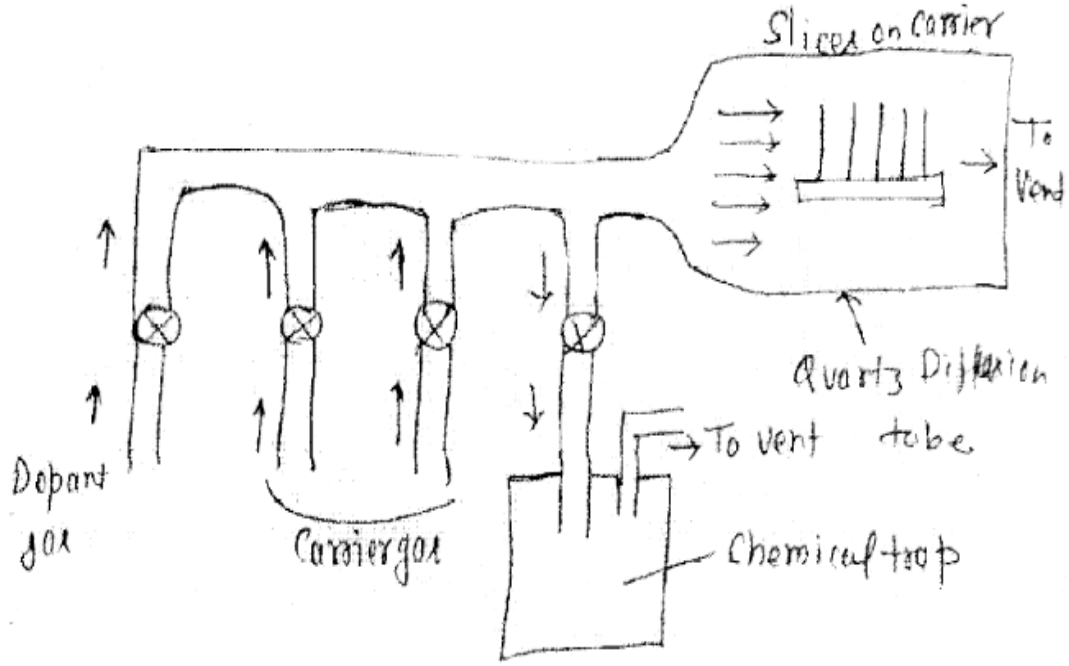
Where:

- $C(x,t)$ is the concentration at position $x$ and time $t$,
- $C0$ is the initial concentration,
- $\delta$ is the depth of diffusion as given by the equation above.

This solution represents the concentration profile as diffusion progresses

**Q7. Explain the gaseous source diffusion system. AKTU-2016-17**

**Ans.**

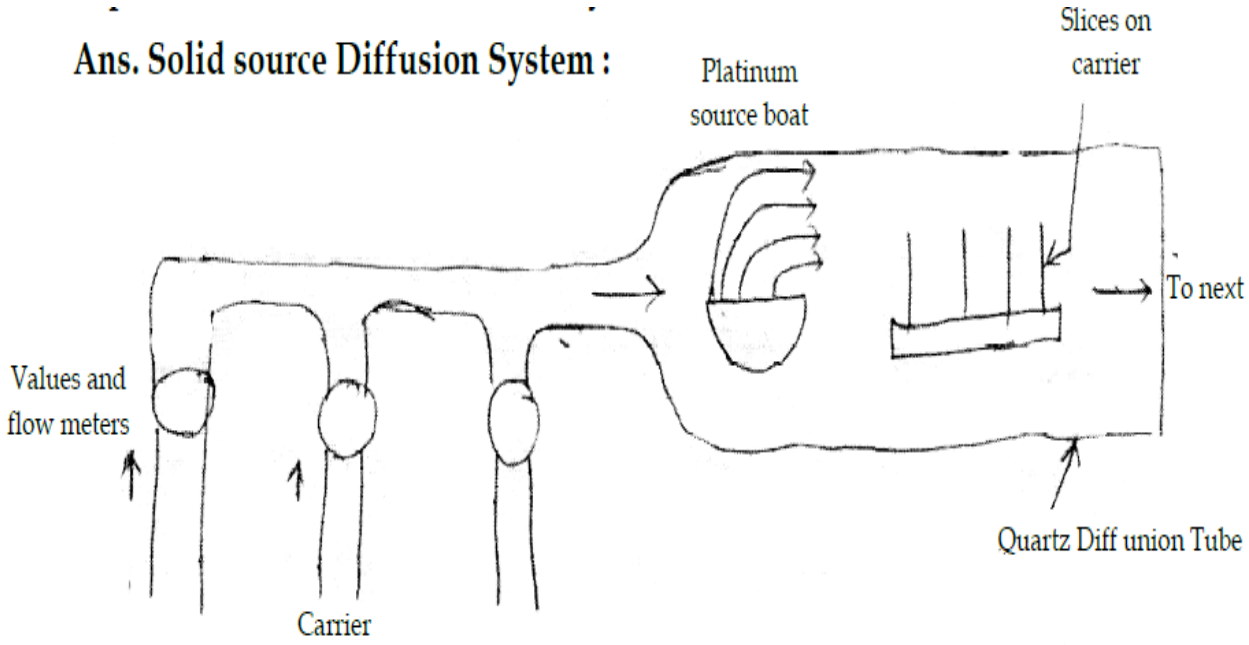



**Gaseous- source diffusion system**

Gaseous source Diffusion system: Gaseous sources are more convenient than liquid source system. It is generally to use an excess dopant gases concentration so that these system are relatively insensitive to gas-flow rate. In gaseous source diffusion system provision is made for an ambient carrier carrier gas in which the diffusion takes place. A chemical trop is opten in corporated to disposed of unreacted dopant gas. The major drawback of the gas source diffusion system is that it is difficult to maintain doping uniformity over all the silicon waters during a diffusion run and even over the surface area of each individual water. This is the due to the depletion occur during transport of the reactant vapoure between water.

**Q8. Explain the solid source diffusion system?**

**Ans. Solid source Diffusion System :**




**Solid source diffusion system**

The circuit arrangement for the solid source diffusion system shown in figure above.In this system we can use aplatinum boat to hold a solid source of depent species upstream from the carrier with semi conductor wafers. In operation the carrier gas transports vapours from. This source and deposits them on the silicon water. Source shut off is usually accomplished by moving the dopant source to a colder region of the source. The source boat and the slices can be maintained at the same temperature avoiding the need for a two zone furnace.

**Q9. Explain solid square diffusion of Boron.**

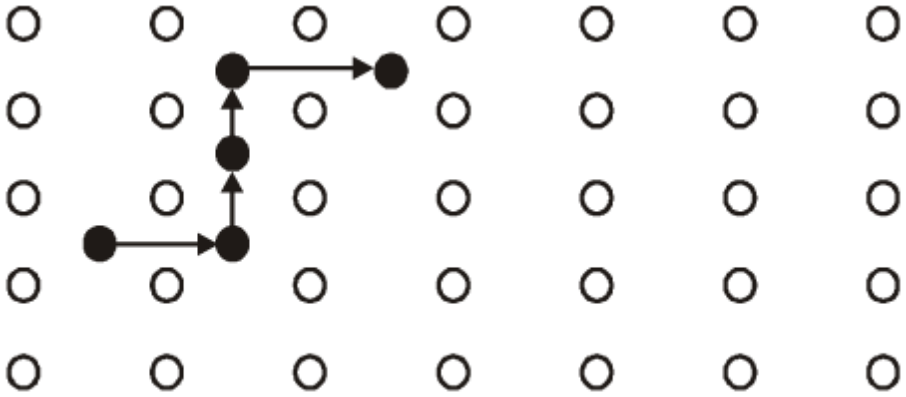
**Ans.** Boron has an intrinsic diffusivity of about 10–22 cm2 s–1 at 12000C. It has a high solid solubility and can be diffused with a surface concentration as large as large 4×1020 atom cm3. In open tube method for B2O3, the source B2O3 isloated on to the diffusion tube and the water are placed in a fig with the polished surface to be doped facing the walls. At the water surface it reacts with surface oxides to forms boro silicate glass which later acts as the source for predisposition. Boron diffusion in accomplished by means of a surface reaction between boron trioxide (B2O3) and the silioon is given by

$$2B_2O_3 + 3Si \rightleftharpoons 4B + 3SiO_2$$

**Q10. What is Diffusion? Explain different type of diffusion? AKTU-2015-16**

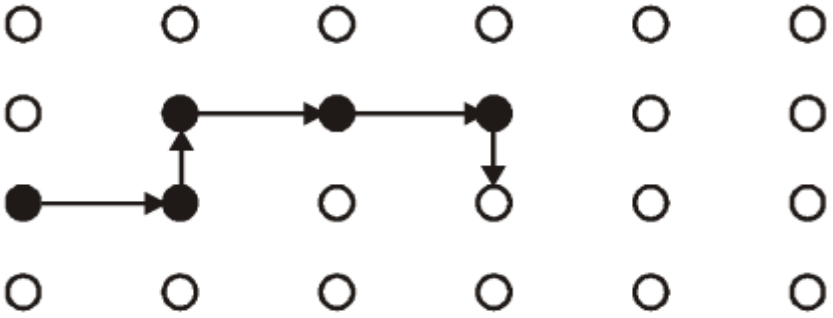
**Ans.** Diffusion : The process by which the atoms move in the crystal lattice is diffusion.The movement of an impurity in a latic takes place in a series of random jumps in all three dimensions and flux of diffusing species results if there is a conentration gradient. Different type of Diffusion.

**(i) Interstitial Diffusion :** In Interstitial diffusion the impurity atoms move through crystal lattice by jumping from one interstyfied site to the next. Interstitial diffusion requloes that their jump motion occurs from one interstitials site to other adjoient site. This type of diffusion can also occur by a dissociatiue mechanism.



Interstitial diffusion of atom

**(ii) Substitutional Diffusion :** In this case, the impurity atom move through the crystal by jumping from one lattice site to the next. In this way they substitute for the original host atom. The presence of vacancies is must for substiutional diffusion.



Substitiotional diffusion

**Q11.What do you mean by sheet resistane? AKTU-2015-16**

**Ans.** Sheet resistane is measure of resistance of thin films that are nominally uniformin thickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition, restive paste printing. The utility of sheet resistane as opposed to resistance or resistivity is that it is directly measured using a four therminal sensing measurement.
Consider a rectangular layers of diffused material of length 'l', width 'w' and thickness 't' so the

$$R = \frac{P_d}{t}\frac{l}{w}$$

.

Pd = specific resistivity of material
This equation may be written as

$$R = R_s \frac{l}{w}$$

where Rs is sheet resistance of diffusion layer. If we take a square layer sheet then the sheet resistane

$R_s = \frac{P_d}{t}$ in unit of ohm per square.

**Q12. What is Importance of Ion Implantation for VLSI Technology? AKTU-2021-22**

**Ans.**

Ion implantation is a very popular process for VLSI because it provides more precise control of dopants (as compared to diffusion). With the reduction of device sizes to the submicron range, the electrical activation of ion-implanted species relies on a rapid thermal annealing technique, resulting in as little movement of impurity atoms as possible. Thus, diffusion process has become less important than methods for introducing impurity atoms into silicon for forming very shallow junctions, an important feature of VLSI circuits. Ion, implantation permits introduction of the dopant in silicon that is controllable, reproducible and free from undesirable side effects. Over the past few years, ionimplantation has been developed into a very powerful tool for IC fabrication. Its attributes of controllability and reproducibility make it a very

versatile tool, able to follow the trends to finer-scale devices. Ion implantation continues to find new applications in VLSI technologies

**Q13. Compare ion implantation process with diffusion?**

**Ans.** Diffusion and ion implantation are two methods of introducing impurities to semiconductors (Silicon - Si) to control the majority type of the carrier and the resistivity of layers. In diffusion, dopant atoms move from surface into Silicon by means of the concentration gradient. It is via substitutional or interstitial diffusion mechanisms. In ion implantation, dopant atoms are added forcefully into Silicon by injecting an energetic ion beam. Diffusion is a high-temperature process while ion implantation is a low-temperature process. Dopant concentration and the junction depth can be controlled in ion implantation, but it cannot be controlled in the diffusion process. Diffusion has an isotropic dopant profile whereas ion implantation has an anisotropic dopant profile.

**Q14. What are the advantage and disadvantage of ion implantation over diffusion process? AKTU-2021-22**

**Ans.**

In diffusion, particles are spread through random motion from higher concentration regions to regions of lower concentration. Ion implantation involves the bombardment of the substrate with ions, accelerating to higher velocities.

**Advantages:** Diffusion creates no damage and batch fabrication is also possible. Ion implantation is a low-temperature process. It allows you to control the precise dose and the depth. Ion implantation is also possible through the thin layers of oxides and nitrides. It also includes short process times.

**Disadvantages:** Diffusion is limited to solid solubility and it is a high-temperature process. Shallow junctions and low dosages are difficult the process of diffusion. Ion implantation involves an ad ditional cost for annealing process.

Diffusion has an isotropic dopant profile whereas ion implantation has an anisotropic dopant profile.

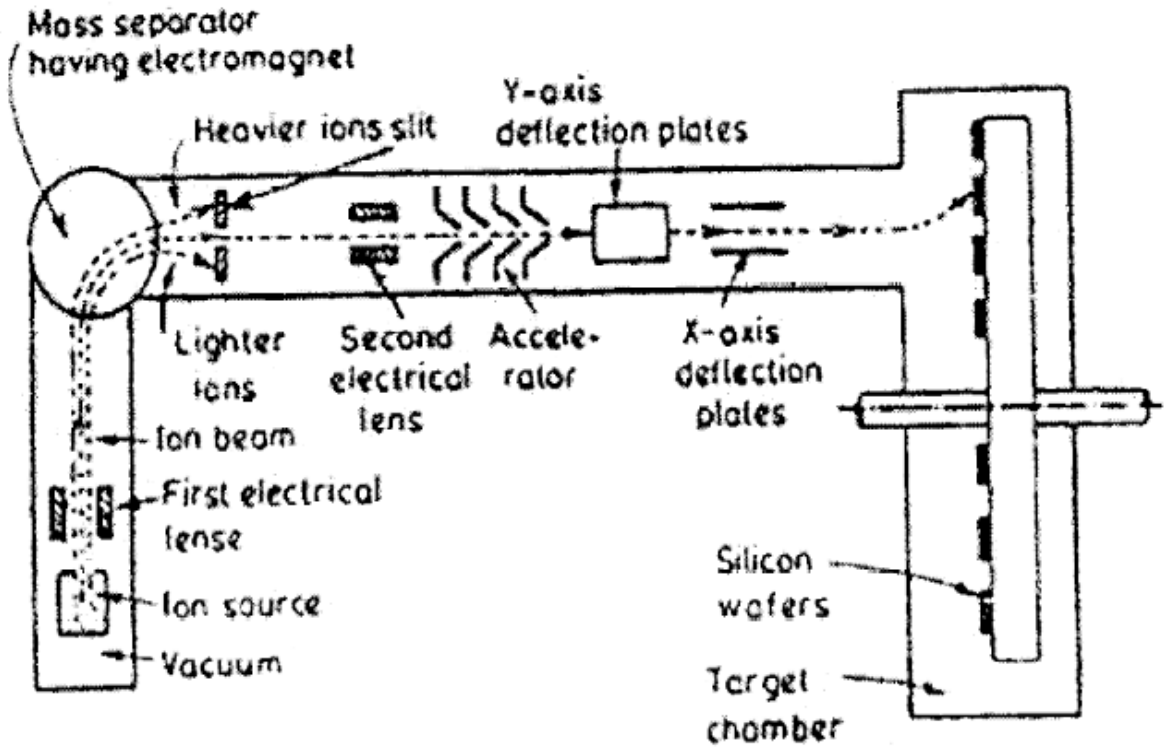
**Q15. Explain Ion-implantation system. AKTU-2021-22,22-23**

**Ans.**

Ion Implantation is an alternative to a deposition diffusion and is used to produce a shallow surface region of dopant atoms deposited into a silicon wafer. This technology has made significant roads into diffusion technology in several areas. In this process a beam of impurity ions is accelerated to kinetic energies in the range of several tens of kV and is directed to the surface of the silicon. As the impurity atoms enter the crystal, they give up their energy to the lattice in collisions and finally come to rest at some average penetration depth, called the projected range expressed in micro meters. Depending on the impurity and its implantation energy, the range in a given semiconductor may vary from a few hundred angstroms to about 1 micro meter. Typical distribution of impurity along the projected range is approximately Gaussian. By performing several implantations at different energies, it is possible to synthesize a desired impurity distribution, for example a uniformly doped region.

A gas containing the desired impurity is ionized within the ion source. The ions are generated and repelled from their source in a diverging beam that is focussed before if passes through a mass separator that directs only the ions of the desired species through a narrow aperture. A second lens focuses this resolved beam which then passes through an accelerator that brings the ions to their required energy before they strike the target and become implanted in the exposed areas of the silicon wafers. The accelerating voltages may be from 20 kV to as much as 250 kV. In some ion implanters, the mass separation occurs after the ions are accelerated to high energy. Because the ion beam is small, means are provided for scanning it uniformly across the wafers. For this purpose the focussed ion beam is scanned electrostatically over the surface of the wafer in the target chamber. Repetitive scanning in a raster pattern provides exceptionally uniform doping of the wafer surface. The target chamber commonly includes automatic wafer handling facilities to speed up the process of implanting many wafers per hour.

A typical ion-implantation system is shown in the figure below.




Ion implantation system

**Q16. Why the acceleration tube has a bend on one end in an ion implantation machine? AKTU-2021-22,16-17**

**Ans. Ion Implantation:**

As we know, the conductivity of the semiconductor increases when small impurity is added to it. The process of adding impurity is called doping while the impurity to be added is called dopant. So ion implantation is a process of adding dopant to the silicon substrate. The ion implantation process is controllable, reproducible and also there are no unwanted side effects. The ion implantation process is prefered over diffusion because of following reasons.

1. the impurity concentration is highly uniform typically within 1%, over the wafer,
2. the degree of uniformity is maintained same from wafer to wafer,
3. the layer can be formed any-where within substrate,
4. the lateral spread is very small.

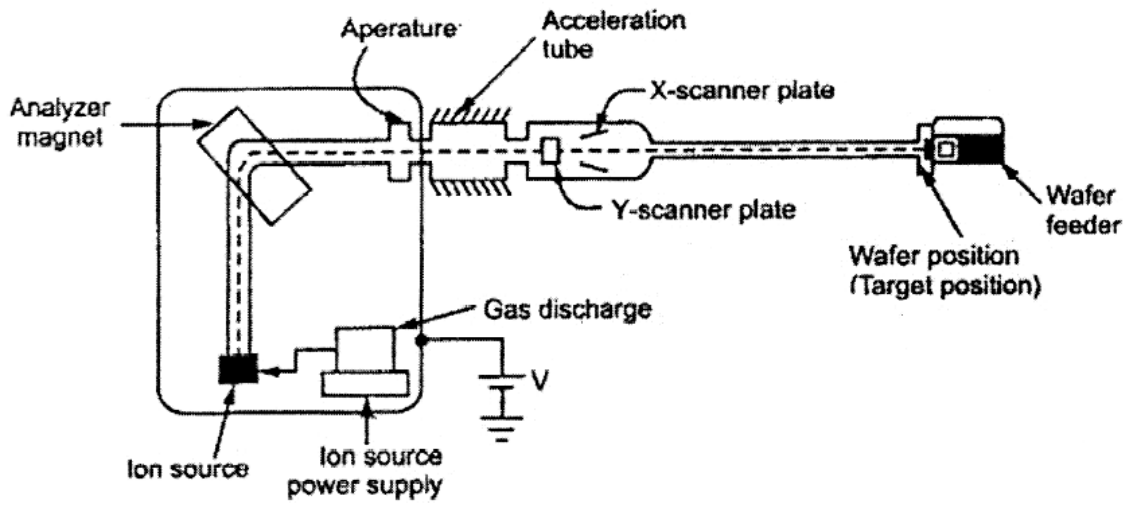



**Fig.: Schematic diagram of typical ion-implanter**

Basically the ion implantation process is low temperature process. In this process, the dopant atoms are vapourized. They are accelerated by an accelerator and then bombarded on silicon substrate. The entire wafer or selected part of it, is exposed to the beam of vapourized, accelerated dopant atoms. The beam injects the dopant atoms into unmasked sections of the substrate. The depant atoms directly enter the crystal lattice of the silicon. In the lattice, due to the collisions with silicon atoms the dopant atoms starts loosing energy. When the energy is totally lost, the dopant atoms are found at some depth within the lattice itself. The depth of penetrations is controlled by the acceleration energy of the incident beam and the doping concentration. In general, the ion implantation is made through thin oxide, as compared to masking which is made through thicker layer of oxide. The main objective of the basic ion implantation is to direct a beam of dopant atoms with the appropriate acceleration and energy to' the silicon substrate. The schematic diagram of a typical ion-implanter is as shown in the Fig. aperture, acceration tube, X-Y scanner plates, target chamber. There are two distinct parts of the system namely high voltage chamber consisting number of system components producing desired ions, while other one is target chamber consisting wafer holding and feeder assemby. A gas source delivers a small amount of gas into the ion source. The gas used is BFa.

There are molecules break into charged particles due to the heating filament. Now in the ion source, there are desired ions along with other charged particles. Due to the high voltage (about 20 kV), the charged ions are pulled out of the ion source into the bending magnet analyzer. Note that the pressure in the system is maintained very low (of the order of 10'6 Torr) so as to avoid scattering of ions due to gas molecules. The bending analyzer magnet selects the ions with desired charge to mass ratio with the help of properly applied magnetic field. Thus the desired ions only can travel through the analyzer, while the others impinge on the analyzer walls. In the acceleration tube, the ions are accelerated to the suffeciently high implantation energy

The aperture focusses the beam of ions. The X-Y scanner plates adjust the sweep of the beam over the wafer placed in target chamber. The wafer is slightly offset to the axis of the acceleration tube so as to avoid deflection of ions on to the wafer. In typical ionimplanter, accelerator voltages range from few kV to 250 kV for medium energy implanters, while upto 2 MV for high energy implanters. Typically a medium energy implanter is 6m long, 3m wide and 2 m high. It process 200 wafers per hour. The total number of ions enetering the target is called dose. The medium energy implantation dosage extends from about $^{1010to}$ $10^{17}$ atoms/cm2.

# UNIT-05

**Q1. What is sputtering? AKTU-2022-23**

**Ans.** In this technique, we have a big target material. Metal source is usually a big disc. The target material is bombarded by energetic ions. So, from the target material some material is pulled out by the force. After that the material is condensed on the substrate to form the film of the metal.

**Q2. What is ohmic contact in VLSI?AKTU-2022-23**

**OR**

**Why is metallization done? AKTU-2021-22**

**Ans.** It is the process by which components of the ICs are interconnected by metal usually aluminum. Metal contact is the connection of integrated circuit to the outside world.Ohmic Contact Metallization simply forms ohmic contacts.

**Q3. What is the disadvantage of Sputtering? AKTU-2021-22**

**Ans.** Disadvantage of Sputtering is that, this process damages the surface of the substrate if the ions have high energy.

**Q 4. Why is aluminum preferred for metallization?? AKTU-2021-22**

**Ans.** The use of aluminium offers the following advantages.

1. It has relatively good conductivity.
2. It is easy to deposit the thin film of aluminium by vacuum evaporation.
3. It has good adherence to the silicon dioxide surface.
4. It has good mechanical bond with silicon.

**Q5. Mention various packaging types available for IC fabrication.AKTU-2021-22**

**Ans. Following packaging types available for IC fabrication**

a. Package Types

b. Packaging Design Consideration
c. VLSI Assembly Technologies

**Q6. Explain the metallization and describe the problems associated with this process. Explain dc sputtering method of metallization? AKTU-2022-23**

**Ans** • Initially, we have metal in solid form.
• We have form this metal into gas or vapor.
• After getting metal in gaseous form, transport it to the target where we want to deposit the metal.
• Finally, the metal which is in gaseous form, it must be condensed back as a film on the target.
• So, there are 3 steps for deposition of metal.
1. Convert solid metal in gas/vapor. 2. Transport it to the target.
3. Condensation of vapor/gas and growth of the film.

**Problem associated with Metallization**

• There are basically 2 problems associated with metallization.
1. Junction spiking
2. Electro-migration

**Sputtering method of metallization**

In this technique, we have a big target material. Metal source is usually a big disc. The target material is bombarded by energetic ions.So, **Physical Etching** takes place.So, from the target material some material is pulled out by the force. After that the material is condensed on the substrate to form the film of the metal.

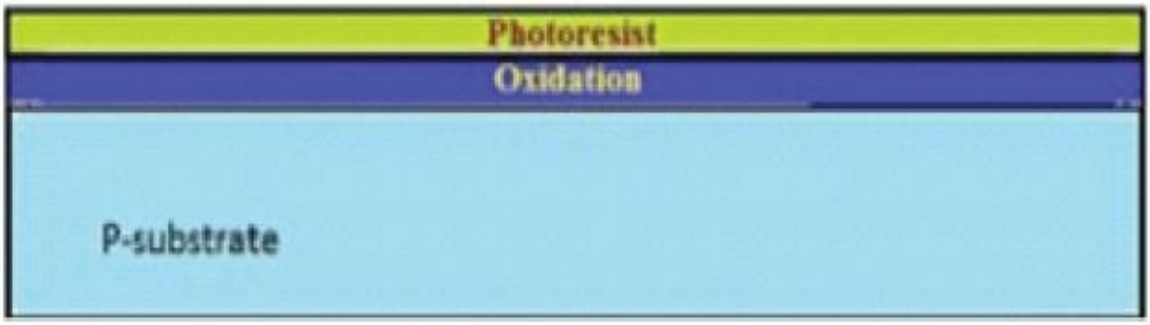
• **Advantages** of this technique is that it has capability of cleaning the substrate prior to metal deposition.
• **Disadvantage** is that, this process damages the surface of thesubstrate if the ions have high energy.

**Q7. Explain CMOS fabrication steps in detail?. AKTU-2022-23,21-22,21-21,19-20**

**Ans.** A P-well has to be created on a N-substrate or N-well has to be created on a P substrate. In this article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.
The fabrication process involves twenty steps, which are as follows:
Step1: Substrate
Primarily, start the process with a P-substrate

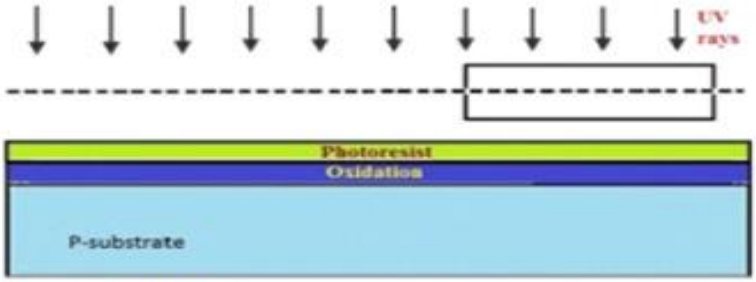

**Step2: Oxidation**
The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade


**Step3: Photoresist**
A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed



**Step4: Masking**

The photoresist is exposed to UV rays through the N-well mask

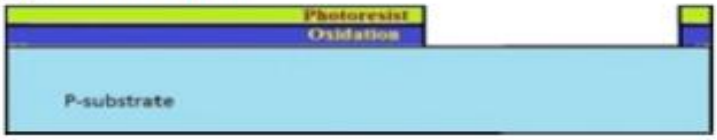



**Step5: Photoresist removal**

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.


**Step6: Removal of SiO2 using acid etching**

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.

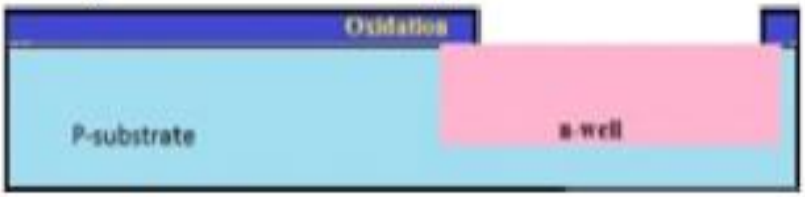



**Step7: Removal of photoresist**

The entire photoresist layer is stripped off, as shown in the below figure.

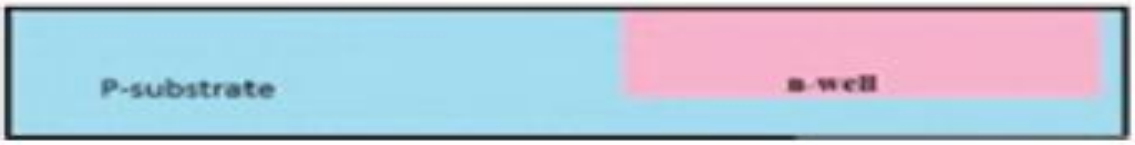

**Step8: Formation of the N-well**

By using ion implantation or diffusion process N-well is formed.




**Step9: Removal of SiO2**

Using the hydrofluoric acid, the remaining SiO2 is removed.

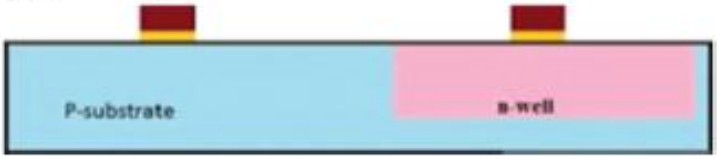



**Step10: Deposition of polysilicon**

Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.

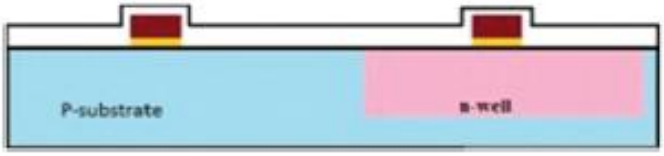

**Step11: Removing the layer barring a small area for the Gates**

Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



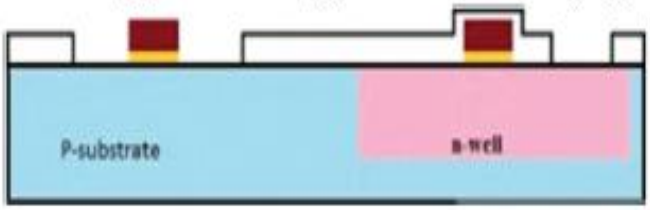

**Step12: Oxidation process**

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.

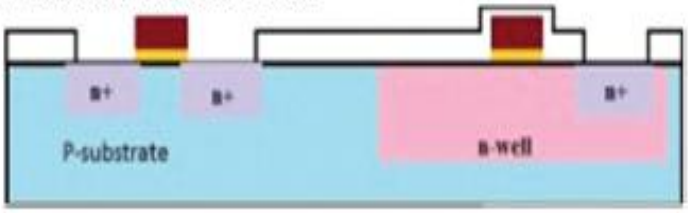



**Step13: Masking and N-diffusion**

By using the masking process small gaps are made for the purpose of N-diffusion.

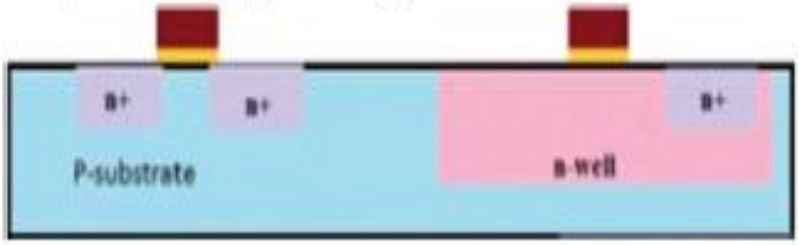



The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.



**Step14: Oxide stripping**

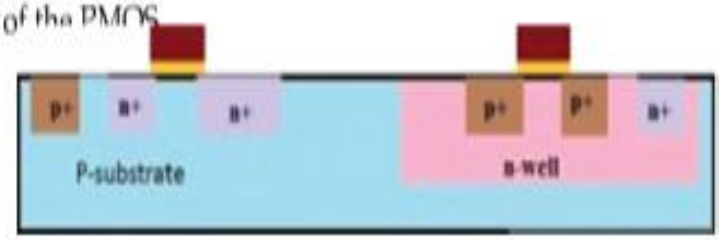
The remaining oxidation layer is stripped off.




**Step15: P-diffusion**

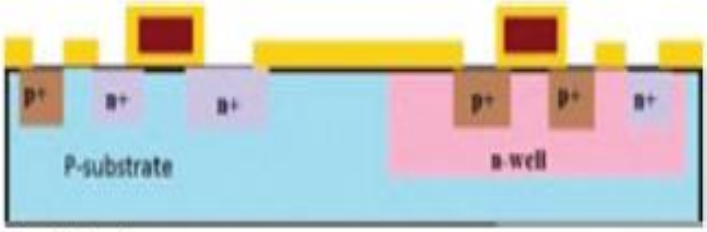
**Step15: P-diffusion**

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



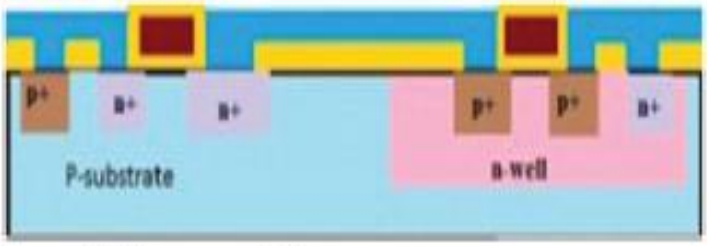

**Step16: Thick field oxide**

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.



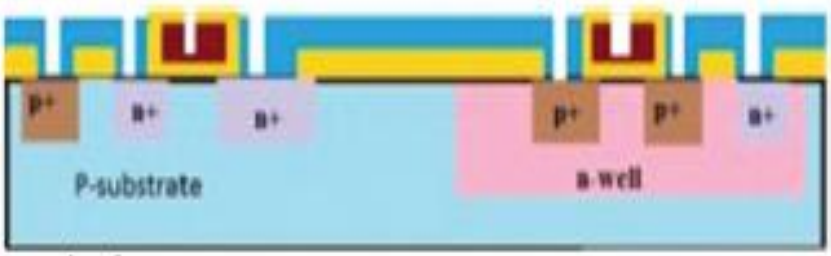

**Step17: Metallization**

Aluminum is sputtered on the whole wafer.



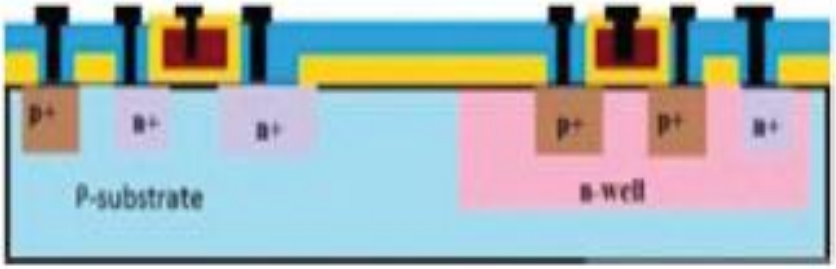
**Step18: Removal of excess metal**

The excess metal is removed from the wafer layer.

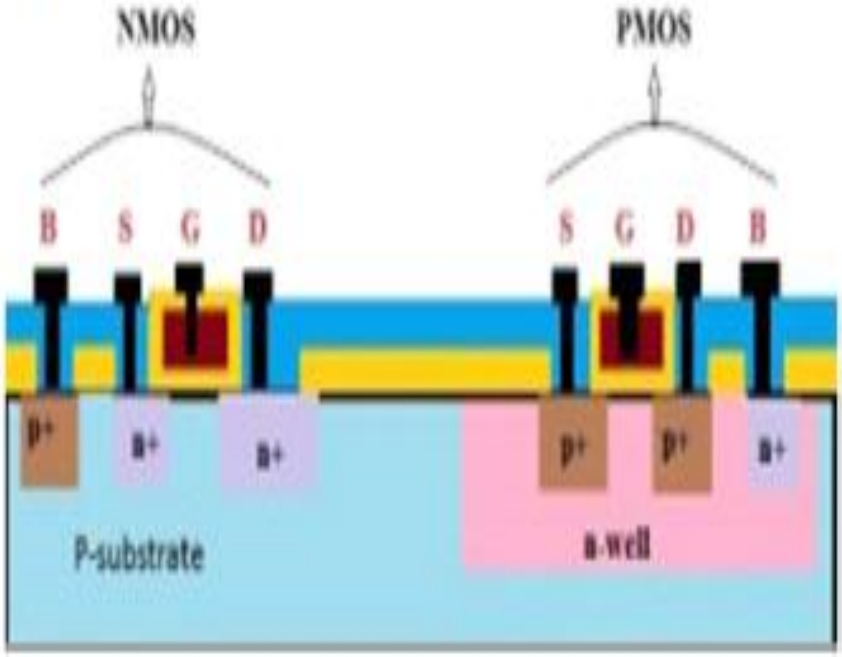



Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.




Step20: Assigning the names of the terminals of the NMOS and PMOS



Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS. P-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices

**Q8. Briefly explain Vacuum Deposition and Sputtering for metallization? AKTU-2021-22,20-21**

**Vacuum Evaporation Technique of metallization**

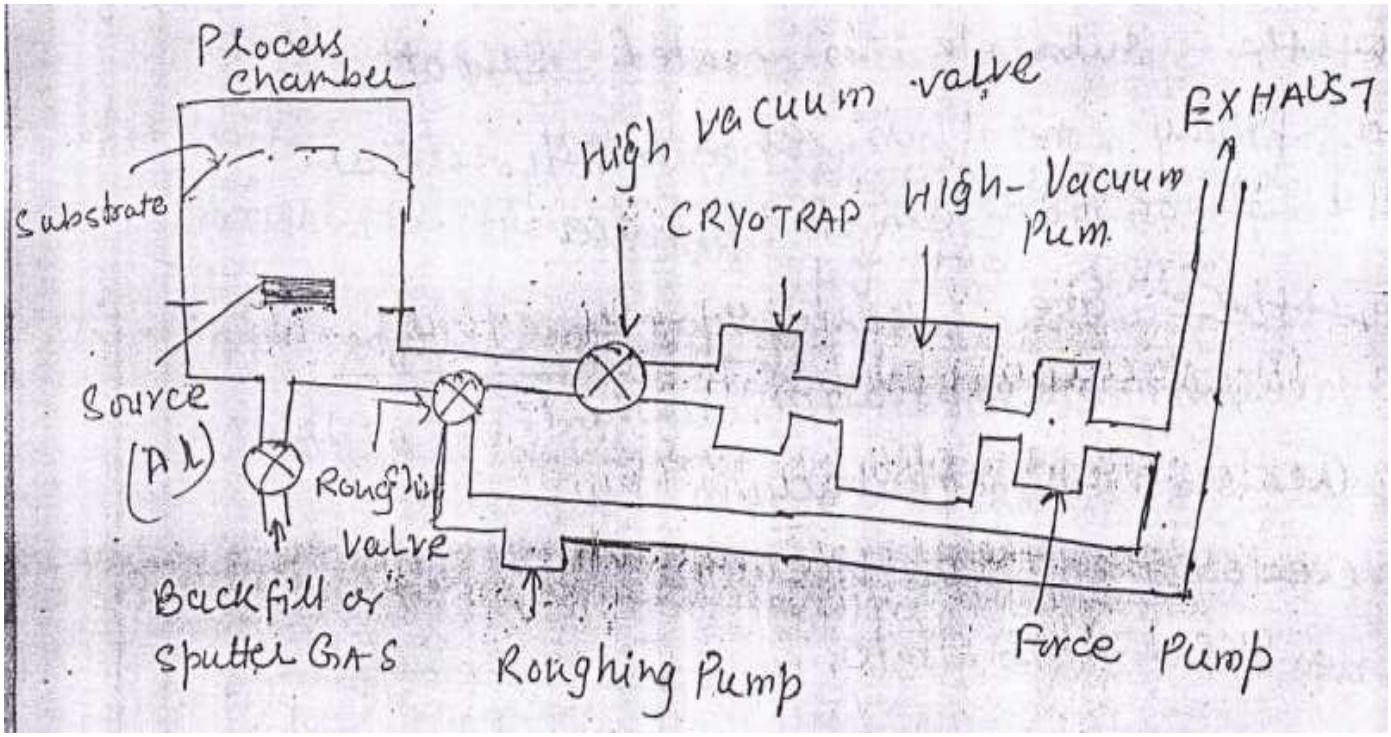



Fig: Vacuum Evaporation Chamber for metal deposition

Initially we have a substrate which is kept at a lower temperature. The metal source is placed at a heater. Then we heat the metal source, the metal forms the vapor. As the substrate is at lower temperature it condenses (Vapor) on the substrate. E – Beam Technique is used if the metal has very high melting point. Vacuum Evaporation Chamber for metal deposition has shown on previous slide.Chamber has gas/air inlet. We have a combination of pumps. Roughing pump is used to create the rough vacuum. High vacuum pump

along with cryotrap and force pump is used to create high vacuum. Source (metal) is placed inside the chamber. When we open the inlet valve and roughing valve, the roughing pump creates the rough vacuum. After the rough vacuum has been achieved, open the high vacuum valve. Now the substrate is heated slightly. And finally metal is evaporated so that metal deposition can take place. So, there are basically 4 steps in Vacuum Evaporation technique

1. Create the rough vacuum

2. Create the high vacuum

3. Heat the substrate

4. Evaporation of metal

**Q9. What are the disadvantages of using Aluminum for metallization? How are they rectified? AKTU-2021-22**

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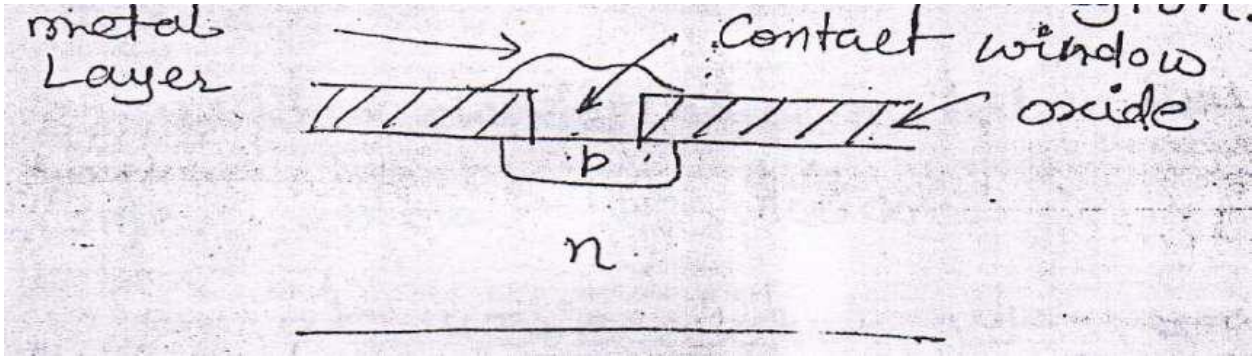
**Ans.** There are basically 2 problems associated with metallization

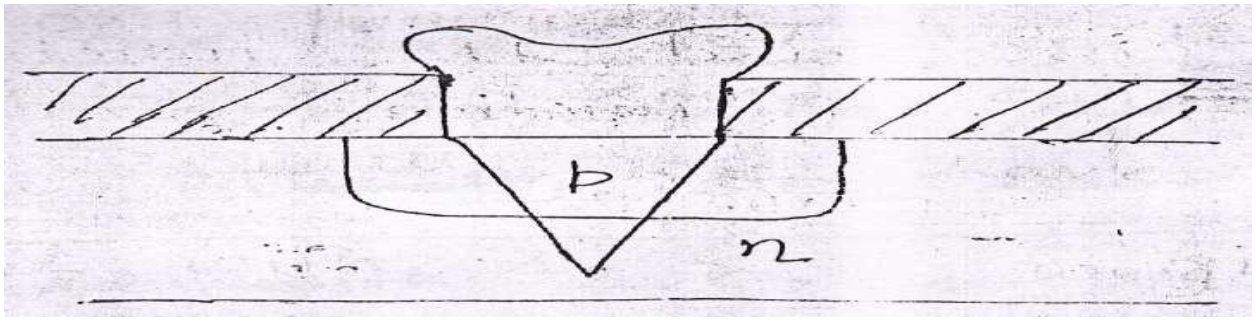
1. Junction spiking
2. Electro-migration

**1. Junction Spiking**

Let we have a p-n junction.



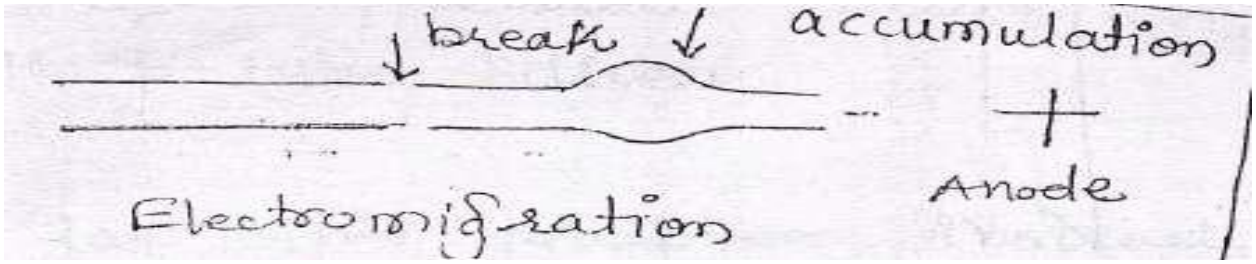

We put metal on p region. At 450 0C, Aluminium dissolves 0.5% of Silicon by weight.If the contact window is smaller and the junction is shallow, then there is possibility of junction spiking.




Now the question is "How to reduce the problem of junction spiking". Initially during metal deposition, don't deposit the pure aluminum. Aluminium must have little bit of silicon mixed. So the deposited metal has already some amount of silicon. When at 450 0C, when it starts to dissolve 0.5% of Silicon, the silicon is supplied from the Aluminium itself. It doesn't need to take silicon from substrate. So, one possibility is that the metal must contain some amount of silicon.Usually we have, Al with Si > 1 weight %.

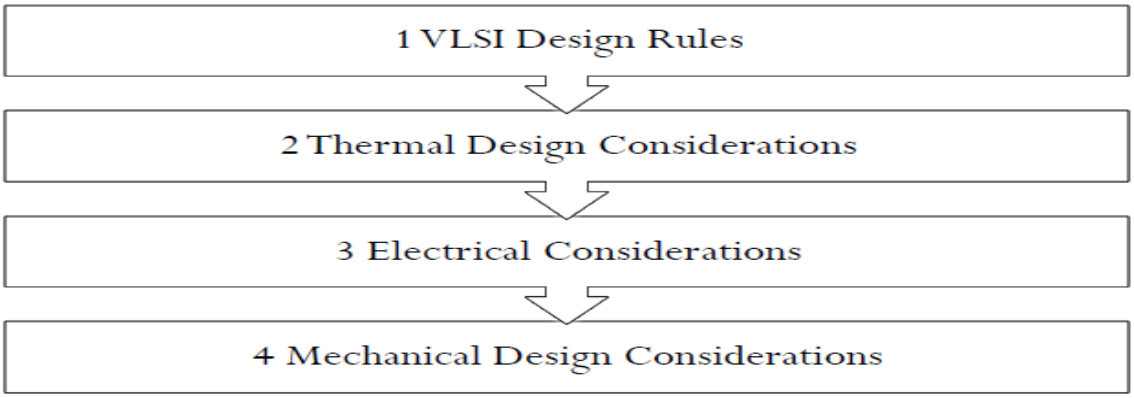
**2. Electromigration**

We have metal lines & electrons carrying current. Electrons are moving under the influence of electric field. The higher the electric field, the faster will be the movement of electrons.Due to movement of electrons, they may collide with +ve metal ions & transfer momentum to the metal ions. If the sufficient momentum is transferred, then the actual metal ions also starts moving towards the direction of the anode.Because electrons move towards the anode So, due to electromigration there is break in the metal along with accumulation of metal along with accumulation of metal towards the direction of anode.So, it is physical transfer of metal from one place to another place under the influence of electric field, this is called electromigration. • Electromigration can be reduced by using aluminium with copper.



**Q10. What are the different package types used for VLSI devices? What are different packaging design considerations?? AKTU-2020-21**

**Ans.** Packaging Design Consideration

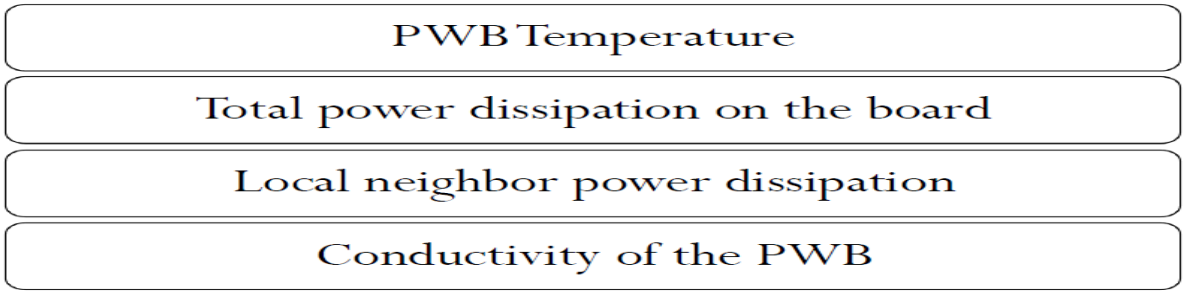



**1. VLSI Design Rules**

In order to achieve high yields in VLSI package assembly establishment of good chip design rules is essential. Rules must be different for particular package type. The rules must be compatible with assembly equipment. As the I/O count grows and the active VLSI device size shrinks, the bonding pad size and spacing (pitch) should be reduced. Figure shows consequence of increasing I/Os on the bonding pad pitch for several chip sizes. Reliability and the ability to assemble VLSI chips is affected by the chip layout.

**2. Thermal Design Considerations**

The operating junction temperature of a silicon die must be as low as possible to prevent the failure rates.The heat is transferred from die to surface of the package (case) by conduction and from the package to the ambient by convection and radiation. Usually the temperature difference between the case and ambient is small so the radiation can be neglected.The packaged device environment must be established for the following variables.



The overall thermal resistance can be considered as the sum of two thermal resistance components *θjc and θca, where*

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \ (^{o}C/Watt)$$

$$\theta_{jc} = [T_j - T_c]/P$$

$$\theta_{ca} = [T_c - T_a]/P$$

- Where
  - $\theta_{ja}$ = junction to ambient thermal resistance
  - $\theta_{jc}$ = junction to case thermal resistance
  - $\theta_{ca}$ = case to ambient thermal resistance
  - $T_j$ = average die or junction temperature ($^{o}C$)
  - $T_c$ = average case temperature ($^{o}C$)
  - $T_a$ = ambient temperature ($^{o}C$)
  - P = power (Watts)

**3. Electrical Considerations**

In IC packaging level, there are several electrical performance criteria.

- Low ground resistance (minimum power supply voltage drop)
- Short signal leads (minimum self inductance)
- Minimum power supply spiking due to signal lines simultaneously switching
- Short paralleled signal runs near a ground plane (minimum capacitive loading)
- Maximum use of matched impedances to avoid signal reflection.
  All of the avobecriteria depends upon some variables such as;
- conductor cross section
- conductor length
- dielectric thickness
- dielectric constant of packaging body.
- The most important electrical consideration in IC packaging is noise reduction.
- When a line switches the voltage induced in the ground line is given be;

  **Vi= Lg di/dt**

  Where
- Viis induced voltage
- Lgis the inductance of the ground lead
- di/dtis the derivative of the current with respect to time.

- If j lines are switching, then Viis given by;

$$V_i = L_g \Sigma \, di_j/dt$$

So in order to reduce Vimultiple grounds must be used to reduce Lg.If m ground leads are used, the total inductance will be Lg/m.The inductance can be reduced through the use of large ground planes within the package

**4: Mechanical Design Considerations**

The material for package construction ideally match physical properties of the VLSI die usually TCE (Thermal Coefficient Expansion). In actual design, the die is attached using materials like solder, alloy or adhesive. During the packaging process the heat may melt solders. So Alloy 42 (Fe-Ni 42%) is used, it has poor thermal conductivity, but closely matches the TCE of silicon. Mechanical reliability requires a good matching between the thermal properties like the TCE of the integrated circuit and the package. Hermetic packages offer high degree of matching, because no package materials comes in direct contact with IC surface.

## Q11. VLSI Assembly Technologies? AKTU-2020-21

**Ans.** Process of electrically connecting I/O bond pads on the IC.

- It enables an IC to be electrically interconnected to the package.
- The first step is the preparation of the wafer.
- The second step is the die attach. In this step the die is attached to the package.
- The third step is the wire bonding, which is the process of connecting the bond pad to the lead of the package.
- The fourth step is to encapsulate the die. In this step the die is closed from the interference of external contaminant and protecting from damage etc.
- The fifth step is to seal the package.
- The sixth step is Molding in which the device is encapsulated in plastic material.
- The last step is to test the packaged device.

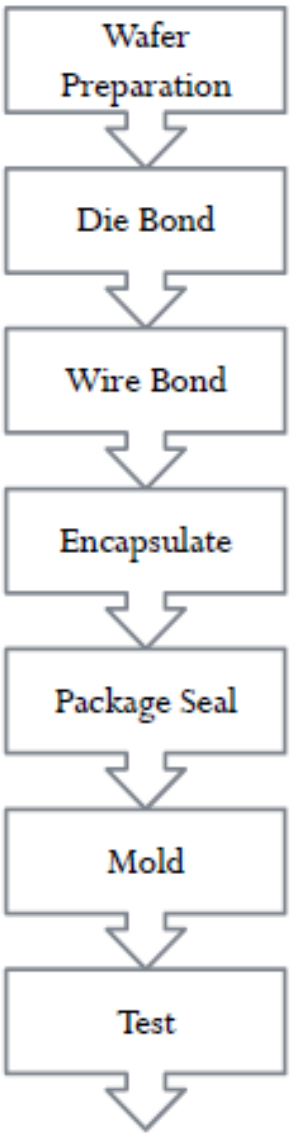



Figure: Generic assembly sequence for plastic and ceramic packages

**Q12. What are Requirement for Metallization? AKTU-2021-22**

**Ans.**

- Low resistivity
- Easy to form
- Easy to etch for pattern generation
- Mechanically stable
- Smooth surface
- Should be stable towards high temperature
- Should not contaminate the wafer
- Reliable & good life time